DEC STD 030-1
MODULE MANUFACTURING STANDARD - GENERAL PRODUCIBILITY REQUIREMENTS

DOCUMENT IDENTIFIER: A-DS-EL00030-01-0 Rev E, - -1990

ABSTRACT: This section of DEC STD 030 provides general rules and guidelines for making early design decisions. It also provides the review and approval process required by Corporate Producibility Engineering to ensure that a new module, power supply, or backplane is produced at the lowest possible manufacturing cost and that volume deliveries will be made within the shortest time cycle.

APPLICABILITY: This standard is mandatory for designs to be compatible with the standard volume manufacturing process. Site Producibility Engineers are available to provide additional information on specific areas not covered in this standard.

STATUS: FOR REVIEW ONLY

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	Rev E	- -1990	ECO Number CTS04

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Responsible Department: Applied Module/PWB Technology (AMPT) Producibility
Responsible Person: Kathy Bailey

APPROVAL: This document has not yet been approved.

Kathy Bailey, Standard Owner

Eric Williams, Standards Process Manager

Direct requests for further information to:

Kathy Bailey

NIO/P19, DTN: 285-2716, SALEM::BAILEY_K

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 287-3724.

1 OVERVIEW OF THE CORPORATE PRODUCIBILITY ENGINEERING SYSTEM

The producibility review and approval process is intended to ensure that a new module, power supply, or backplane is produced at the lowest possible manufacturing cost and that volume deliveries are made within the shortest cycle time.

Exhibit 1 is a Producibility contact matrix. Exhibit 2 shows the consultation and approval functions performed by Producibility in the overall process of product design selection, review, and approval.

A testability review shall be part of the overall producibility process to ensure proper trade-offs between product design and standard test procedures; see *DEC STD 030-6 Module Manufacturing Standard - Module Testability Rules*. Refer to *DEC STD 016-0 Printed-Wiring Manufacturing Terminology* for definitions of terms.

Exhibit 1: Producibility Contact Matrix

Computer Systems Manufacturing (CSM)	Corporate Manager Corporate Advisor	George Beckner Charlie Newell	DELNI::BECKNER RUTLND::NEWALL
Applied Module/ PWB Technology (AMPT)	Standards and Tools	Kathy Bailey	SALEM::BAILEY
	Supervisor	Ed Blair	WONDER::BLAIR
	Intermediate Systems Business (ISB)	Bill Barton Harry Parkinson SteveWash	HPSTEK::BARTON BARNUM::PARKINSON HPSTEK::SWASH
	Computer Special Systems (CSS)	Harry Parkinson	BARNUM::PARKINSON
	Power Supplies	Dennis Anderson	COBRA::ANDERSON
GSG, CSS, TAN	Manager	Joanne Cattley Brian Finneron Bob Dubois	KNGBUD::CATTLEY KNGBUD::FINNERON KNGBUD::DUBOIS
Mid–range Systems	Engineering Manager	Pete Vargus	NISYSG::VARGUS
Storage Systems:	East West	Chris Sweeny Joe Jaramillo	MPGS::SWEENY COMET::JARAMILLO
Low–end Systems Manufacturing (LESM)	Manager	Russ Raby Roy Batcheider John Graham Tim Torode Bob Morawiak Vash Varandari	FRSBEE::RABY FRSBEE::BATCHELDE FRSBEE::GRAHAM FRSBEE::TORODE FRSBEE::MORAWIAK FRSBEE::VARANDARI
Europe	TAN	Sean Linehan Dan Philpot	KLO::LINEHAN KLO::PHILPOT
	ESASE	Mike Fahey	ESASE::FAHEY
Memories	Assigned per product.		

2 PRODUCIBILITY REVIEW AND APPROVAL PROCESS

2.1 PURPOSE OF REVIEW AND APPROVAL PROCESS

The purpose of the producibility review and approval process is to identify any nonstandard design features that may require special action prior to layout. Therefore, this review shall be performed in the design concept stage, prior to the beginning of a lab breadboard. Exhibit 2 shows the overall review and approval process.

2.2 REVIEW/APPROVAL RULES

RULE 1000: REVIEW AND APPROVAL OF NEW DESIGNS

New modules and backplanes shall be reviewed by Producibility using the appropriate Pre-Design Producibility Questionnaire (PDQ) form. See subhead 2.2.1 for ordering information. A sample form is shown in Exhibit 3.

RULE 1010: REVIEW AND APPROVAL OF ECOS TO EXISTING DESIGNS

ECOs to existing modules or backplanes shall be reviewed by Producibility using the Change Design Questionnaire (CDQ) form. See subhead 2.2.1 for sample forms and ordering information. Exhibit 2 shows the overall review and approval process. A sample form is shown in Exhibit 4.

RULE 1020: GRANDFATHER CLAUSE

All modules, power supplies, and backplanes shall meet the requirements of the most current revision of DEC STD 030 in effect at the time the module is released to manufacturing; however, every effort should be made to update these designs to current standards if an ECO is required.

ECOs for the complete re-layout of a module must include plans to update that module to the latest revision of DEC STD 030. In most cases, minor revisions to these modules, such as etch cuts and a few wire adds, will not require an update of the entire module. Contact Producibility for further information.

2.2.1 Pre-Design Questionnaire (PDQ) and Change Design Questionnaire (CDQ) Forms

Automated PDQ and CDQ Forms shall be used for modules and backplanes and are available through the Producibility Automation and Cost Estimator (PACE) software or from Site Producibility Engineers. See Exhibit 3 and Exhibit 4 for sample forms, and heading 7 for further information on PACE.

2.2.2 General Descriptor Code (GDC)

The GDC that is assigned to the new module or backplane is developed from the responses to the PDQ review. The responsible design engineer may fill in the GDC using the example and the code legend shown in Exhibit 5, or may obtain assistance from the Producibility personnel indicated on the PDQ form.

An approximation of the cost to produce a new module or backplane may be obtained through PACE .

Exhibit 2: Flowchart Showing Standard Design Selection, Review, and Approval Process for New or Existing Products

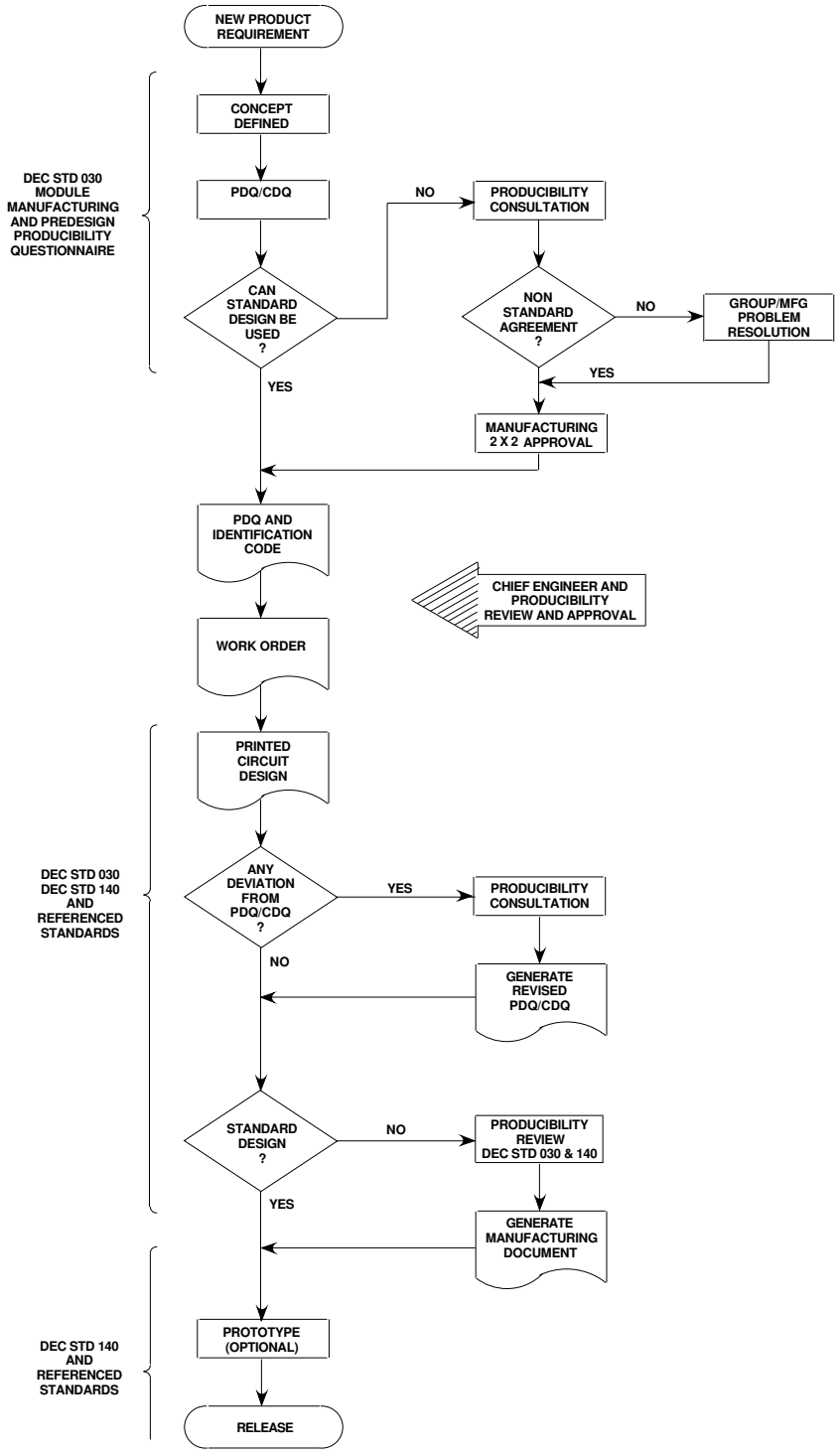


Exhibit 3: Automated PDQ Form

********** F O R D I G I T A L I N T E R N A L U S E O N L Y **********

PDQ Header - PDQ No. REV Date

ENGINEER DTN: Enet: Brd. No:
DSN : Assy No:
PDY : Assy No:
SPME: Assy No:
SPMM: Assy No:
Assy No:

Mfg Group: GD Code:

Option :
Title :

PWB Design Site: FVS : Q FY
PWB Fab Site : Vol/Yr :
Assembly Site : Life Vol:
50 lev rel date: Actual: Etch rev at rel:

DESIGN DATA				SMT DATA	
Family	:			Actives side 2?	:
Size	: x	x		Mimimum pitch	:
PWB technology	:			SMT leads	:
Layers	:	Board Finish	:	Test pts side 1	:
Board technology	:	Solder Mask	:	side 2	:
Line Impedance	:	Smask Type	:		
Outline Code	:	Laminate	:	EICs	:
Circuit Area	:	Foil	:	%MAX	= %
Finger Gold Area	:	Planar Layers	:	PTH Pins	:
Number of Fingers	:	Via Grid	:	Pins/Sq.In	:
Extra Gold Area	:	LBVs	:		
UL Safety	:	Bur. Sig Vias	:	Auto S&R? (Y/N)	:
Min Hole Size	:	Bur. Pad Vias	:		
Nomenclature	:	PWB Title	:		
Stored PWB	:				
PWB UNIT COST	$				

Description of PWB Design Codes

Nomenclature	Solder Mask	Laminate	Foil
0. None	1. None	0. User defined	1. Std Copper
1. One Side	2. One Side	1. Standard (FR-4)	2. HTE Foil
2. Two Sides	3. Two Sides	2. Tetra Epoxy	
	4. Standard	3. BT Epoxy	
		4. Polymide	
		5. Cyanate ester	

Solder mask type		Board Finish
0. None	3. Wet film photo imageable	1. Tin Lead
1. Dry film	4. Optional	2. SMOBC
2. Wet film screened		3. Bare Copper

Exhibit 3 Cont'd on next page

Exhibit 3 (Cont.): Automated PDQ Form

```
       COST DATA (Cost calculated at $55 an hour burdened labor rate)
            PTH                              SMT                        OPERATIONS
       qty  hours   cost              qty  hours   cost              hours   cost
Auto   :          $          Side 1  :          $          PTH     :       $
Hand   :          $          Side 2  :          $          SMT     :       $
Final  :          $          Sbttl   :          $          USER D  :       $
Misc   :          $
Sbttl  :          $          USER D  :          $          TEST    :       $

Number of part nos   :
Total Parts          :
Stored Test Process  :
Stored Parts List    :
Test Process Title   :                        Parts List Title:

PWB        : $           Total Material  : $            UNIT COST      : $
Component  : $           Total Assembly  : $            LIFE VOLUME    :
Comp. w/o cost:          Total Test      : $            EST LIFE COST  : $

ADDITIONAL INFORMATION:
 Any special PWB notches?       :      S&R:           ckts/               bd.
 Pads only outer layer?         :      Technology Defn     :
 Standard grid testability?     :
 Standard component placement?  :      Layer Const dwg     :
 1 oz. copper inner layers OK?  :      Layup               :
 Enter AutoThieving Type.       :
 Will all components, switches,        Circuit outline     :
 connectors, staked pins and           Assembly Board dwg  :
 cables be mounted on side 1?   :

 All components qualified?      :
 Test strategy reviewed?        :

                Charge number   :

NON-STANDARD DESIGN ISSUES/REVISION HISTORY:

PDQ No.         ECO Revision History

Date                 :
System ID            :
User Name            :
Revision No.         :

Reason for Revision  :
```

Exhibit 4: Automated CDQ Form

********** F O R D I G I T A L I N T E R N A L U S E O N L Y **********

CDQ Header - CDQ No. REV Date

ENGINEER DTN: Enet: Brd. No :
DSN : Assy No :
PDY : Assy No :
SPME : Assy No :
SPMM : Assy No :
Assy No :

Mfg Group : GD Code :

Option :
Title :

PWB Design Site : FVS : Q FY
PWB Fab Site : Vol/Yr :
Assembly Site : Life Vol :
50 lev rel date: Actual: Etch rev at rel :

DESIGN DATA SMT DATA

Family	:				Actives side 2?	:
Size	:	x	x		Mimimum pitch	:
PWB technology	:				SMT leads	:
Layers	:		Board Finish	:	Test pts side 1	:
Board technology	:		Solder Mask	:	side 2	:
Line Impedance	:		Smask Type	:		
Outline Code	:		Laminate	:	EICs	:
Circuit Area	:		Foil	:	%MAX	= %
Finger Gold Area	:		Planar Layers	:	PTH Pins	:
Number of Fingers	:		Via Grid	:	Pins/Sq.In	:
Extra Gold Area	:		LBVs	:		
UL Safety	:		Bur. Sig Vias	:	Auto S&R? (Y/N)	:
Min Hole Size	:		Bur. Pad Vias	:		
Nomenclature	:		PWB Title	:		
Stored PWB	:					
PWB UNIT COST	$					

Description of PWB Design Codes

Nomenclature	Solder Mask	Laminate	Foil
0. None	1. None	1. Standard (FR-4)	1. Std Copper
1. One Side	2. One Side	2. Tetra Epoxy	2. HTE Foil
2. Two Sides	3. Two Sides	3. BT Epoxy	
	4. Standard	4. Polymide	
		5. Teflon	

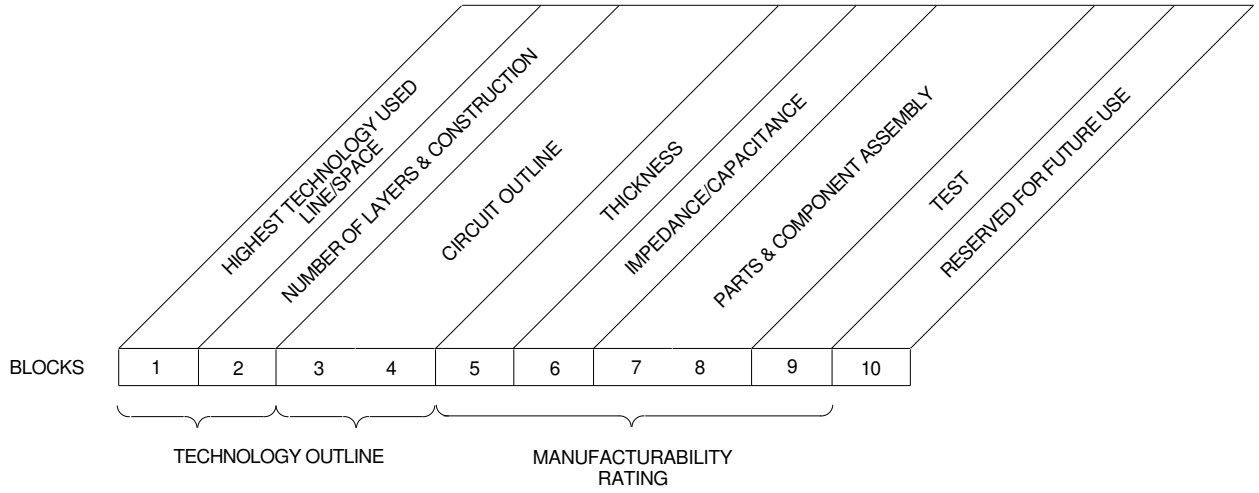
Exhibit 4 Cont'd on next page

Exhibit 4 (Cont.): Automated CDQ Form

```
        COST DATA (Cost calculated at $55 an hour burdened labor rate)
             PTH                              SMT                        OPERATIONS
        qty  hours   cost                qty  hours   cost                  hours   cost
Auto    :           $          Side 1    :           $          PTH        :       $
Hand    :           $          Side 2    :           $          SMT        :       $
Final   :           $          Sbttl     :           $          USER D     :       $
Misc    :           $
Sbttl   :           $          USER D    :           $          TEST       :       $

Number of part#s      :
Total Parts           :
Stored Test Process   :
Stored Parts List     :
Test Process Title    :                          Partslist Title:

PWB              : $        Total Material  : $          UNIT COST       : $
Component        : $        Total Assembly  : $          LIFE VOLUME     :
Comp. w/o cost   :          Total Test      : $          EST LIFE COST   : $

ADDITIONAL INFORMATION:
 Any special PWB notches?        :      S&R:            ckts/                bd.
 Pads only outer layer?          :      Technology Defn      :
 Standard grid testability?      :
 Standard component placement?   :      Layer Const dwg      :
 1 oz. copper inner layers OK?   :      Layup                :
 Standard Auto Thieving OK?      :
 Will all components, switches,         Circuit outline      :
 connectors, staked pins and            Assembly Board dwg   :
 cables be mounted on side 1?    :
 Is this module a backplane?     :

 All components qualified?       :
 Test strategy reviewed?         :

                 Charge number   :
```

```
                                                          (Y/N/NA)

    Will the board size/outline remain the same?           :
    Will the number of layers remain the same?             :
    Will components be moved during relayout?              :
    Any new parts to be qualified?                         :
    Will the test strategy change?                         :
    Does the UL rating change?                             :
    Will UL frame be updated to current STD.?              :
    Will all currently waived items be corrected?          :



NON-STANDARD DESIGN ISSUES/REVISION HISTORY:

CDQ# CX9558     ECO Revision History


Date                  :
System ID             :
User Name             :
Revision #            :

Reason for Revision   :
```

Exhibit 5: General Descriptor Code (GDC) Development and Code Legend



SEE GDC CODES LEGEND FOR DEFINITIONS

BLOCK 1: HIGHEST TECHNOLOGY USED—LINE/SPACE		
A = P/G plane	J =	T =
B = 20/20 SD	K = SMOBC 20/20	U = pads outer layers 15/15
C = 15/15 HD1	L = SMOBC 15/15	V = pads only 12/13
D = 12/13 HD2	M = SMOBC 12/13	W = pads only 8/8
E = 8/8 FL1	N = SMOBC 8/8	X = pads only 6/10
F = 6/10 FL2 and FL3	P = SMOBC 6/10	Y = pads only 5/5
G = 5/5 FL4	R = SMOBC 5/5	Z =
H =	S =	

BLOCK 2: NUMBER OF LAYERS		
A = 1	K = 10	V = 28
B = 2 non PTH	L = 12	W = 30
C = 2 PTH	M = 14	X = 32
D = 4	N = 16	Y = 34
E = 6 pads outer layers	P = 18	Z = 36
F = 6	R = 20	1 = 38
G = 8 pads outer layers	S = 22	2 = 40
H = 8	T = 24	3 = 42
J = 10 pads outer layers	U = 26	4 = 44

Exhibit 5 Cont'd. on next page

Exhibit 5 (Cont): General Descriptor Codes

BLOCKS 3 AND 4 : OUTLINE—01 THROUGH 99 AND NS

01 = 5-inch single	27 = 4-inch x 5.2-inch FICS
02 = 8.5-inch single	28 = 4-inch x 10.4-inch FICS
03 = 5-inch dual	29 = 3.2-inch x 1.3-inch FICS
04 = 8.5-inch dual	30 = 3.2-inch x 2.6-inch FICS
05 = 5-inch quad	31 = 3.2-inch x 5.2-inch FICS
06 = 8.5-inch quad	32 = 3.2-inch x 10.4-inch FICS
07 = 8.5-inch hex	33 = 2-inch x 1.3-inch FICS
08 = 12-inch hex - M-series	34 = 2-inch x 2.6-inch FICS
09 = 16-inch x 5.2-inch SGF	35 = 2-inch x 5.2-inch FICS
10 = 16-inch x 10.4-inch SGF	36 = 2-inch x 10.4-inch FICS
11 = 8-inch x 5.2-inch SGF	37 = 1.6-inch x 1.3-inch FICS
12 = 8-inch x 10.4-inch SGF	38 = 1.6-inch x 2.6-inch FICS
13 = 4-inch x 5.2-inch SGF	39 = 1.6-inch x 5.2-inch FICS
14 = 4-inch x 10.4-inch SGF	40 = 1.6-inch x 10.4-inch FICS
17 = 16-inch x 1.3-inch FICS	91 = 10.436-inch x 8.160-inch - T-3000 series
18 = 16-inch x 2.6-inch FICS	92 = 15.688-inch x 11.91-inch P-series 1050 to 1068
19 = 16-inch x 5.2-inch FICS	93 = 10.436-inch x 4.91-inch - L-series
20 = 16-inch x 10.4-inch FICS	94 = 10.436-inch x 8.40-inch - L-series
21 = 8-inch x 1.3-inch FICS	95 = 10.436-inch x 10.6-inch - L-series
22 = 8-inch x 2.6-inch FICS	96 = 9.180 X 11.024-inch T-2000 series
23 = 8-inch x 5.2-inch FICS	97 = 12-inch hex - F-series
24 = 8-inch x 10.4-inch FICS	98 = 9.180 x 8.0-inch T-1000 series
25 = 4-inch x 1.3-inch FICS	99 = 12-inch hex - L-series
26 = 4-inch x 2.6-inch FICS	NS = non-standard size/backplane

BLOCKS 3 AND 4: NON STANDARD FICS SIZES (number of circuits) -AA THROUGH EZ

AA = 1 CKT	BA = 24	CA = 47	EA = EXT.FICS 1 CKT
AB = 2	BB = 25	CB = 48	EB = 2
AC = 3	BC = 26	CC = 49	EC = 3
AD = 4	BD = 27	CD = 50	ED = 4
AE = 5	BE = 28	CE = 51	EE = 5
AF = 6	BF = 29	CF = 52	EF = 6
AG = 7	BG = 30	CG = 53	EG = 7
AH = 8	BH = 31	CH = 54	EH = 8
AJ = 9	BJ = 32	CJ = 55	EJ = 9
AK = 10	BK = 33	CK = 56	EK = 10
AL = 11	BL = 34	CL = 57	EL = 11
AM = 12	BM = 35	CM = 58	EM = 12
AN = 13	BN = 36	CN = 59	EN = 13
AP = 14	BP = 37	CP = 60	EP = 14
AR = 15	BR = 38	CR = 65	ER = 15
AS = 16	BS = 39	CS = 66	ES = 16
AT = 17	BT = 40	CT = 67	ET = 17
AU = 18	BU = 41	CU = 68	EU = 18
AV = 19	BV = 42	CV = 69	EV = 19
AW = 20	BR = 43	CW = 70	EW = 20
AX = 21	BX = 44	CX = 71	EX = 21
AY = 22	BY = 45	CY = 72	EY = 22
AZ = 23	BZ = 46	CZ = 73	EZ = 23

Exhibit 5 Cont'd. on next page

Exhibit 5 (Cont): General Descriptor Codes

BLOCK 5: THICKNESS		MAXIMUM RECOMMENDED LAYERS
A = FR4	0 - .075	8
B = FR4	.076 - .100	14
C = FR4	.101 - .128	TBD
D = FR4	.129 - .150	24
E = FR4	.151 - .175	TBD
F = FR4	.176 - .250	TBD
G = FR4	> .250	Not Recommended
K = POLYIMIDE	.076 - .100	
L = POLYIMIDE	.101 - .128	
M = POLYIMIDE	.129 - .150	
N = POLYIMIDE	.151 - .175	
P = POLYIMIDE	.176 - .250	
R = POLYIMIDE	> .250	Not Recommended
S = BT		

BLOCK 6: PARAMETRIC RATING

A = Nontransmission line
B = Transmission line
G = PRT 1 layer non-transmission (PRT - Planar Resistor Technology)
H = PRT 1 layer transmission
N = PRT 2 layer non-transmission
P = PRT 2 layer transmission

* 1 = Nontransmission line plus laminated-blind vias (LBVs)
* 2 = Transmission line plus LBVs
7 = Nontransmission line plus buried vias
8 = Transmission line plus buried vias

* Not available for volume manufacturing.

Exhibit 5 (Cont): General Descriptor Codes

BLOCKS 7 AND 8

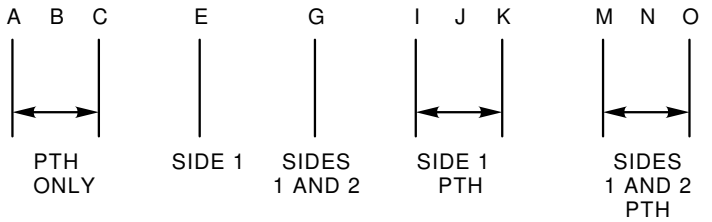
ASSUMPTIONS

Note 1. In this table, it is assumed that a board with hand assembled parts will require either handles or shear. Therefore, from the first inclusion of hand assembly, the shear/handles is assumed. This is a necessary assumption to keep the quantity of different GDC codes at a reasonable number.

Note 2. Serialization of modules is part of the standard process and not optional.

Note 3. Threshold between Final and Final/Complex is based on part count. Part count >5 = Final/Complex.

PROCESS CATEGORY by FIRST–CHARACTER ALPHA CODE



AA = NONE
AB = FINAL ONLY
AC = FINAL ONLY WITH HANDLES
AD = FINAL (COMPLEX) ONLY
AE = FINAL (COMPLEX) WITH HANDLES

BA = HAND ONLY (See Note 1)
BB = HAND + FINAL
BC = HAND + FINAL (COMPLEX)
BD = ECO + HAND ONLY
BE = ECO + HAND + FINAL
BF = ECO + HAND + FINAL (COMPLEX)

CA = VCD + HAND
CB = VCD + HAND + FINAL
CC = VCD + HAND + FINAL (COMPLEX)
CD = VCD + ECO + HAND
CE = VCD + ECO + HAND + FINAL
CF = VCD + ECO + HAND + FINAL (COMPLEX)
CG = DIP, NO VCD + HAND
CH = DIP, NO VCD + HAND + FINAL
CI = DIP, NO VCD + HAND + FINAL (COMPLEX)
CJ = DIP, NO VCD + ECO + HAND
CK = DIP, NO VCD + ECO + HAND + FINAL
CL = DIP, NO VCD + ECO + HAND + FINAL (COMPLEX)

Exhibit 5 Cont'd. on next page

Exhibit 5 (Cont): General Descriptor Codes

BLOCKS 7 AND 8

CM = DIP + VCD + HAND
CN = DIP + VCD + HAND + FINAL
CO = DIP + VCD + HAND + FINAL (COMPLEX)
CP = DIP + VCD + ECO + HAND
CQ = DIP + VCD + ECO + HAND + FINAL
CR = DIP + VCD + ECO + HAND + FINAL (COMPLEX)

EA = SMT SIDE 1 ONLY

GA = SMT SIDE 1 AND SMT SIDE 2

IA = SMT SIDE 1 + FINAL ONLY
IB = SMT SIDE 1 + FINAL ONLY WITH HANDLES
IC = SMT SIDE 1 + FINAL (COMPLEX) ONLY
ID = SMT SIDE 1 + FINAL (COMPLEX) WITH HANDLES

JA = SMT SIDE 1 + HAND ONLY (See Note 1)
JB = SMT SIDE 1 + HAND + FINAL
JC = SMT SIDE 1 + HAND + FINAL (COMPLEX)
JD = SMT SIDE 1 + ECO + HAND ONLY
JE = SMT SIDE 1 + ECO + HAND + FINAL
JF = SMT SIDE 1 + ECO + HAND + FINAL (COMPLEX)
KA = SMT SIDE 1 + VCD + HAND
KB = SMT SIDE 1 + VCD + HAND + FINAL
KC = SMT SIDE 1 + VCD + HAND + FINAL (COMPLEX)
KD = SMT SIDE 1 + VCD + ECO + HAND
KE = SMT SIDE 1 + VCD + ECO + HAND + FINAL
KF = SMT SIDE 1 + VCD + ECO + HAND + FINAL (COMPLEX)
KG = SMT SIDE 1 + DIP, NO VCD + HAND
KH = SMT SIDE 1 + DIP, NO VCD + HAND + FINAL
KI = SMT SIDE 1 + DIP, NO VCD + HAND + FINAL (COMPLEX)
KJ = SMT SIDE 1 + DIP, NO VCD + ECO + HAND
KK = SMT SIDE 1 + DIP, NO VCD + ECO + HAND + FINAL
KL = SMT SIDE 1 + DIP, NO VCD + ECO + HAND + FINAL (COMPLEX)
KM = SMT SIDE 1 + DIP + VCD + HAND
KN = SMT SIDE 1 + DIP + VCD + HAND + FINAL
KO = SMT SIDE 1 + DIP + VCD + HAND + FINAL (COMPLEX)
KP = SMT SIDE 1 + DIP + VCD + ECO + HAND
KQ = SMT SIDE 1 + DIP + VCD + ECO + HAND + FINAL
KR = SMT SIDE 1 + DIP + VCD + ECO + HAND + FINAL (COMPLEX))

Exhibit 5 Cont'd. on next page

Exhibit 5 (Cont): General Descriptor Codes

BLOCKS 7 AND 8

MA = SMT SIDES 1 AND 2 + FINAL ONLY
MB = SMT SIDES 1 AND 2 + FINAL ONLY WITH HANDLES
MC = SMT SIDES 1 AND 2 + FINAL (COMPLEX) ONLY
MD = SMT SIDES 1 AND 2 + FINAL (COMPLEX) WITH HANDLES
NA = SMT SIDES 1 AND 2 + HAND ONLY (See Note 1)
NB = SMT SIDES 1 AND 2 + HAND + FINAL
NC = SMT SIDES 1 AND 2 + HAND + FINAL (COMPLEX)
ND = SMT SIDES 1 AND 2 + ECO + HAND ONLY
NE = SMT SIDES 1 AND 2 + ECO + HAND + FINAL
NF = SMT SIDES 1 AND 2 + ECO + HAND + FINAL (COMPLEX)

OA = SMT SIDES 1 AND 2 + VCD + HAND
OB = SMT SIDES 1 AND 2 + VCD + HAND + FINAL
OC = SMT SIDES 1 AND 2 + VCD + HAND + FINAL (COMPLEX)
OD = SMT SIDES 1 AND 2 + VCD + ECO + HAND
OE = SMT SIDES 1 AND 2 + VCD + ECO + HAND + FINAL
OF = SMT SIDES 1 AND 2 + VCD + ECO + HAND + FINAL (COMPLEX)
OG = SMT SIDES 1 AND 2 + DIP, NO VCD + HAND
OH = SMT SIDES 1 AND 2 + DIP, NO VCD + HAND + FINAL
OI = SMT SIDES 1 AND 2 + DIP, NO VCD + HAND + FINAL (COMPLEX)
OJ = SMT SIDES 1 AND 2 + DIP, NO VCD + ECO + HAND
OK = SMT SIDES 1 AND 2 + DIP, NO VCD + ECO + HAND + FINAL
OL = SMT SIDES 1 AND 2 + DIP, NO VCD + ECO + HAND + FINAL (COMPLEX)
OM = SMT SIDES 1 AND 2 + DIP + VCD + HAND
ON = SMT SIDES 1 AND 2 + DIP + VCD + HAND + FINAL
OO = SMT SIDES 1 AND 2 + DIP + VCD + HAND + FINAL (COMPLEX)
OP = SMT SIDES 1 AND 2 + DIP + VCD + ECO + HAND
OQ = SMT SIDES 1 AND 2 + DIP + VCD + ECO + HAND + FINAL
OR = SMT SIDES 1 AND 2 + DIP + VCD + ECO + HAND + FINAL (COMPLEX))

BLOCK 9: TEST

A = Traditional test
B = Specialized test
C = Traditional and specialized test

BLOCK 10: Reserved for Future Use.

3 WAIVERS TO DEC STD 030

All waivers to the rules of this standard must be obtained by following the procedure outlined in this heading. The procedure in *DEC STD 066-2 Waivers to Digital Design Standards* does not apply. All approved waivers to this standard will be reviewed on a quarterly basis to determine if an ECO to DEC STD 030 is required.

RULE 1030: WAIVERS TO DEC STD 030

Waivers are required for all modules, power supplies, or backplanes that do not comply with the rules of this standard or preliminary agreements documented on the PDQ. Waiver forms are available from Site Producibility representatives and are stored in the central PACE database in the PDP package along with the PDQ and feedback sheet.

Waivers are prepared by the Design Engineer using the form shown in Exhibit 6 and must include the following information.

a. An explanation of the problem and its impact on manufacturing in terms of cost and time

b. If resolution is possible, how and when

c. The date that the engineer will ECO the product to correct the problem, if applicable

d. The quantity of modules to be produced under this waiver

The Design Engineer is also responsible for acquiring the following signatures, indicating acceptance.

a. Engineering Systems Program Manager (or equivalent)

b. Manufacturing Systems Program Manager (or equivalent)

c. Manufacturing Plant Engineer responsible for the product at the location where the product will be built

d. Producibility Engineer

The group Manufacturing Engineer and the DEC STD 030 section owner must also sign the waiver if the Producibility Engineer determines that the module design will have a major impact on manufacturing.

The design engineer has the option of forwarding a rejected waiver to the responsible person for the section of DEC STD 030 to be waived. The responsible person will then present the waiver before the DEC STD 030 Committee with recommendations for approval or rejection. A waiver rejected by the committee cannot be approved through any other procedure.

Exhibit 6: Module Waiver Form

********** DIGITAL INTERNAL USE ONLY **********

MODULE WAIVER FORM

A waiver is required for modules/power supplies/backplanes that do not comply to the rules of DEC STD 030. Waivers are prepared by the design engineer and must include the following information:

PDQ # : Date :
Board No : Etch Rev :
Module No: Module Rev:

STATEMENT OF PROBLEM:

IMPACT TO MANUFACTURING IN TIME/COST:

RESOLUTION (HOW AND WHEN):

QUANTITY OF MODULES TO BE PRODUCED UNDER THIS WAIVER:

REQUIRED APPROVALS:

ENGINEERING SPM (or equivalent)_____ DATE:_____

MANUFACTURING SPM _____ DATE:_____

MANUFACTURING PLANT ENGINEER_____ DATE:_____

PRODUCIBILITY ENGINEER_____ DATE:_____

NO MAJOR IMPACT (Y/N) ____

If the producibility engineer determines that the waiver will have a major impact on manufacturing, the following signatures are also required:

GROUP MANUFACTURING ENGINEER:_____ DATE:_____

DEC STD 030 SECTION OWNER_____ DATE:_____

4 TECHNOLOGY AND CIRCUIT SIZE SELECTION RULES

The following rules must be applied to obtain the most cost-effective product design. PACE can be a useful tool to help select a standard technology and circuit outline. See heading 7 for further information on PACE.

Appendix C provides information on surface mount technology levels. Refer to EL-MF417-02, *Surface Mount Technology Reference Manual - Volume 2*, part 6, subhead 3.2 for descriptions of each technology level. Consult producibility for information regarding availability /startup dates and the use of more advanced features such as double-side actives, 0.010-inch vias, and 0.025-inch pitch components.

4.1 MODULE FAMILY TYPES

Historical Information Listing on Digital Module Family Types	
Green Block Connector Series	5.0-inch, 6.0-inch, and 8.5-inch singles (36 I/Os), doubles (72 I/Os), and quads (144 I/Os); 8.5-inch and 12.0-inch hexes (216 I/Os), fingers at 0.125-inch
A-series	Analog modules (amber handle)
B-series	5mHz logic modules with negative logic for the PDP7[1] (blue handle)
K-series	Very slow industrial modules (black handle)
M-series	Positive logic integrated circuit modules (magenta handle)
R-series	Slow (1 mHz) general purpose modules (red handle)
S-series	Speeded-up R-series (2 mHz) for the PDP8[1]
W-series	Converter modules (negative logic to positive and vice versa, drive relays, and power drivers for high-current applications - white handle)
W 9000 series	Wirewrap modules
G-series	Internal use only, test equipment (green handle)
Y-series	Customer-specific (yellow handle)
X-series	Xerox[2] modules (yellow handle)

Pressed-Pin Connectors	
L-series	Extended hex, 3 sets 0.100-inch fingers (off-grid), 276 I/Os
L-series	(quad by 4.9, 8.4, and 10.6) 2 sets 0.100-inch fingers (off grid) 184 I/Os
C-series	FICS size, 4 sets 0.100-inch fingers (on grid), 296 I/Os

[1]PDP7 and PDP8 are trademarks of Digital Equipment Corporation.

[2]Xerox is a trademark of Xerox Corporation.

ZIF Connectors	
F-series	Extended hex, 2 sets fingers (8 connector sections) 448 I/Os
T-series	Euro-card compatible (5 connector sections) 280 I/Os
T-1000 series	9.180 x 8.000
T-2000 series	9.180 x 11.024
High Density Interconnect	
T-3000 series	10.436 x 8.160
Soldered Connector	
E-series	Extended hex
Right angle connector	
P-1001 through P-1050 series	4-inch by 4-inch high density signal carrier
P-1051 through P-1068 series	15.7 x 11.91 extended hex, 6 rows connector pins, 536 signal and ground, and 5 power pins
H-series	**H3** - Distribution panels, cable assemblies, turnaround connectors and other items used in communication. May contain 54-class parts. **H4** - AC input boxes. May contain 54-class parts. **H7** - Power supplies. May contain 54-class parts. **H8** - Connectors (H803 is the 288-pin green block) **H90 to H949** - Backplanes

4.2 SOLDERMASK OVER BARE COPPER (SMOBC) RULES AND GUIDELINES

Soldermask Over Bare Copper (SMOBC) is a PWB fabrication process resulting in a finished PWB that has solder placed only on solderable terminal areas. All other surface etch features will be bare copper encapsulated with soldermask. SMOBC is the preferred approach for high density/fine line (fine line 1, 2, 3, and 4) surface etch. Although SMOBC may add cost to the PWB, it reduces assembly cost in rework and inspection. Contact Producibility for further information on cost impact.

RULE 1035: USE OF SOLDERMASK OVER BARE COPPER (SMOBC)

Regardless of the etch technology, soldermask must be used on both sides of the board if SMOBC is selected as the manufacturing process. SMOBC shall not be employed if soldermask is applied to only one side. Refer to *DEC STD 140-1 Documentation Requirements for Printed-Wiring Boards, Modules, and Backplanes*.

4.3 TECHNOLOGY CHOICE AND CIRCUIT SIZE SELECTION

Appendix A provides instructions for calculating the maximum number of ICs that can be placed on a printed-wiring board and EIC equivalences. Appendix B provides current carrying capacities for copper thickness and line width.

The standard board thickness families used at Digital are:

0.062 inch 0.093 inch 0.125 inch

Refer to EL-ENPCB-00, *PC Board Engineering Handbook*, for standard thicknesses and layups. Standard thicknesses defined in EL-ENPCB-00 do not include soldermask thickness. The maximum overall thickness of a PWB, including soldermask, is equal to the overall thickness given in EL-ENPCB-00 plus 0.004 inch for each soldermasked layer.

Because of cost implications, each signal layer should have a power or ground plane on the opposite side of the laminate.

Contact Producibility for assistance with nonstandard layups or for materials selection assistance when designing PWBs with planar resistor technology.

NOTE

For machine insertion, the maximum board thickness is 0.100 inch.

RULE 1050: STANDARD PRINTED-CIRCUIT TECHNOLOGY SELECTION

Select a standard printed-circuit technology from <REFERENCE>(techdef_pwbtol_fig_full).

RULE 1060: STANDARD PRINTED-CIRCUIT OUTLINES

Select a standard printed-circuit outline from the following exhibits.

Exhibit 8 Standard 0.125-Inch Finger Circuit Sizes, Side 1 View
Exhibit 9 Standard Fingerless Circuit Sizes (FICS), Circuit Detail Requirements
Exhibit 10 Standard 0.100-Inch Grid Finger Circuit Sizes (SGF)

Exhibit 14 provides a brief description of the detailed drawings referenced in Exhibit 8, Exhibit 9, and Exhibit 10. Ordering information for these drawings is provided in the Referenced Documents section.

RULE 1070: DIGITAL RESTRICTED APPLICATION CIRCUIT OUTLINES

Select restricted application circuit outlines only after interconnection requirements have been approved by Producibility. The following module families require the use of restricted application circuit outlines.

Exhibit 11 Digital L-series Circuit Outline
Exhibit 12 Digital T-series Circuit Outline
Exhibit 13 Digital F-series Circuit Outline

Exhibit 14 provides a brief description of the detailed drawings referenced in Exhibit 11, Exhibit 12, and Exhibit 13. Ordering information for the documents that contain these drawings is provided in the Referenced Documents section.

RULE 1080: TOOLING HOLE LOCATION FOR FICS AND SGF CIRCUITS

The standard position for tooling holes for FICS and SGF circuits is 0.200 inch from the edge of the board. Four tooling holes are recommended. If four tooling holes are not used, see Rule 1085. If standard locations for tooling holes are not used for SGF circuits, see EL-MFPCB1-01.

RULE 1085: CROP MARKS FOR FICS AND SGF CIRCUITS

If a full complement of tooling holes (four) are available in the standard location, in accordance with Rule 1080, crop marks are *not* required for FICS and SGF circuits. If less than four tooling holes are provided, then crop marks will be provided at the corners within the circuit area where tooling holes are not provided. See Exhibit 7.

Crop marks are provided mainly as a visual aid during the shearing process and for visual inspection of circuit edge locations.

Exhibit 7: Crop Marks for FICS and SGF Circuits

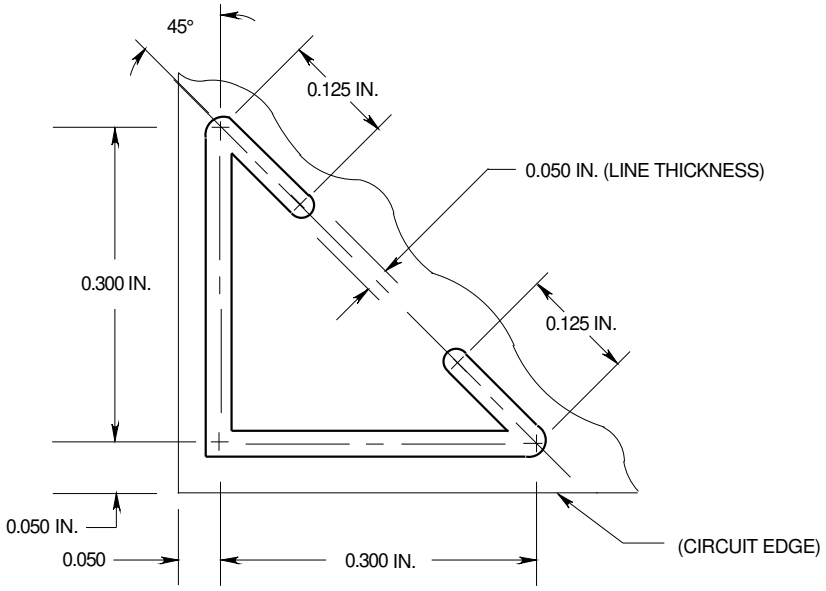
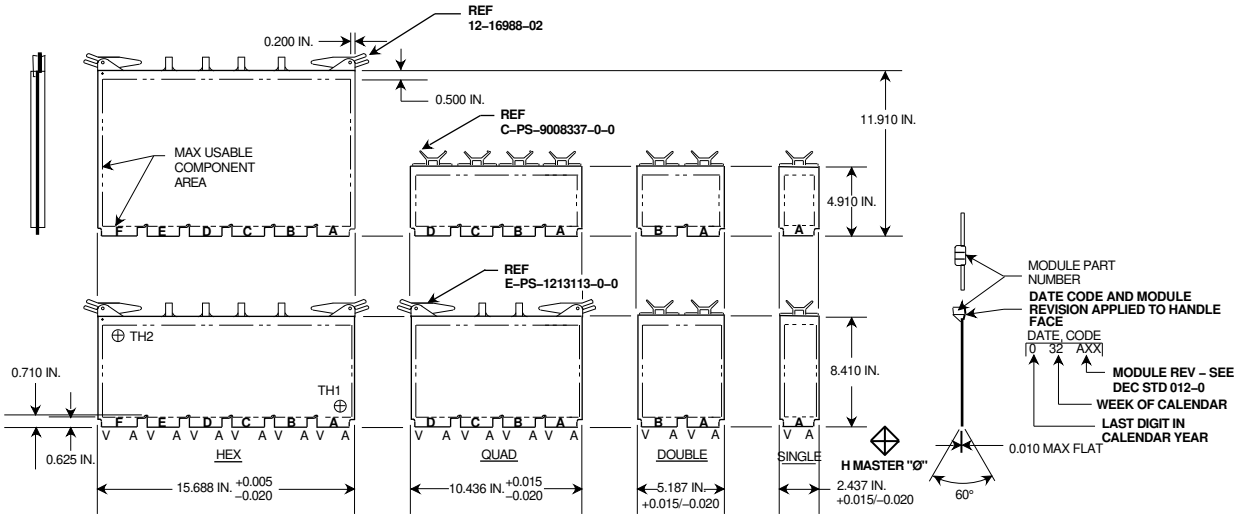


Exhibit 8: Standard 0.125-Inch Finger Circuit Sizes (Green Block Connector Series), Side 1 View

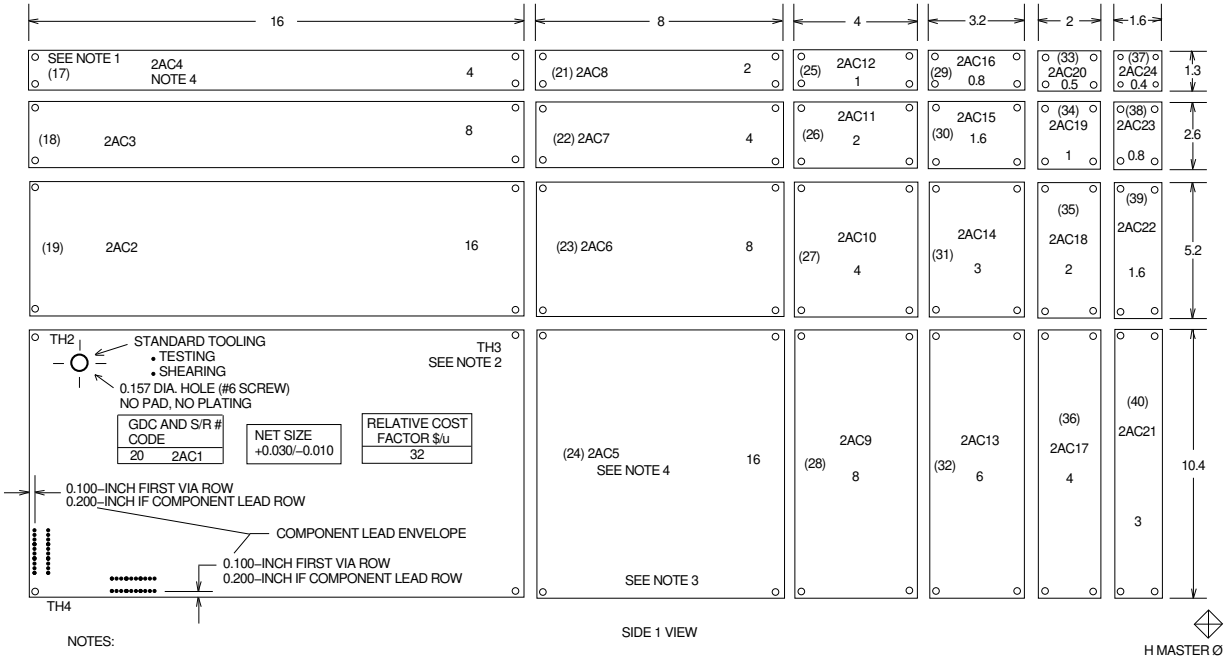


NOTE

1. **⊕ = Recommended location for module tooling holes. See <REFERENCE>(std_refdes_rule_full) and <REFERENCE>(module_testhole_rule_full).**
2. **This drawing is for reference only. Refer to D-MD-ELEN623-0-DBU and D-MD-ELEN652-0-DBU in the PC Board Engineering Handbook for detailed information.**

Refer to subhead 4.1 and Exhibit 14.

Exhibit 9: Standard Fingerless Circuit Sizes (FICS), Circuit Detail Requirements

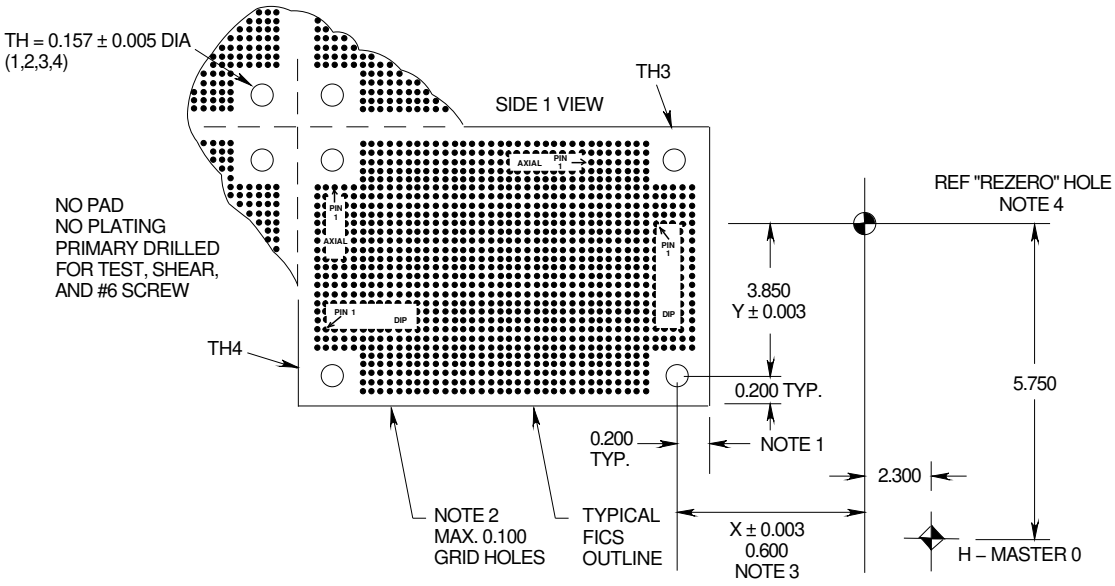


NOTES:

1. ( ) = FICS IDENTIFICATION NUMBER
2. SEE SHEET 2 FOR DIMENSIONS, PROPER DESIGN LOCATIONS, AND ORIENTATION.
3. BREADBOARDS ARE AVAILABLE IN THE ENGINEERING MODEL SHOP.
4. "STEP AND REPEAT" NUMBERS ARE NOT TO BE CONFUSED WITH CIRCUIT SIZE.

Exhibit 9 Cont'd on next page

Exhibit 9 (Cont.): Standard Fingerless Circuit Sizes (FICS), Circuit Detail Requirements



NOTES:

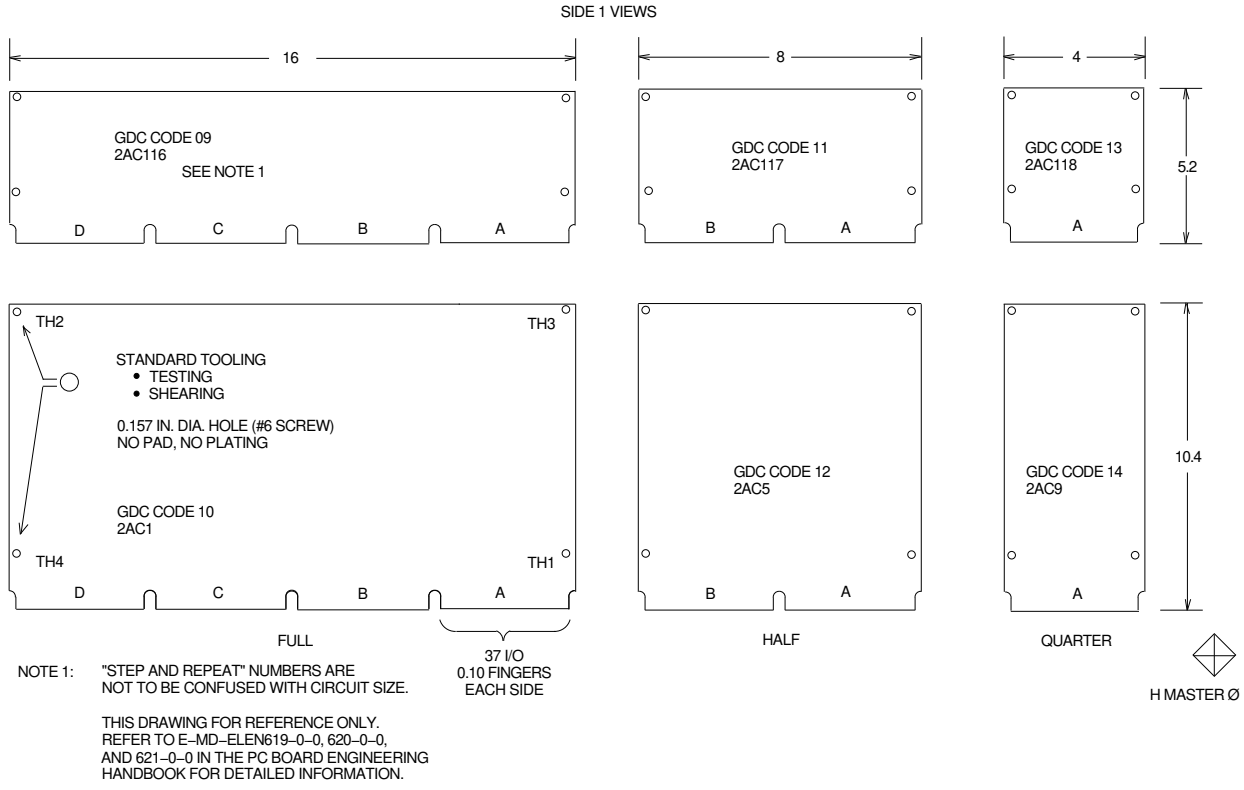
1. NO COMPONENT LEAD WITHIN 0.200 FROM CIRCUIT EDGE. NO COMPONENT BODY WITHIN 0.170 FROM CIRCUIT EDGE.
2. FIRST EDGE ROWS ON FOUR SIDES ARE FOR VIA USE ONLY.
3. LOCATIONS IN DESIGN DATA BASE. THIS LOCATION IS 0.400 INCH ON FINISHED BOARD.
4. REZERO HOLE IS USED FOR A ZERO REFERENCE LOCATION FOR AUTO–INSERTION. SEE DEC STD 176–0.
5. ALL DIMENSIONS ARE IN INCHES.

NOTE

This drawing is for reference only. Refer to D-MD-ELEN623-0-DBU and D-MD-ELEN652-0-DBU in the PC Board Engineering Handbook for detailed information.

Refer to Exhibit 14.

Exhibit 10: Standard 0.100-Inch Grid Finger Circuit Sizes (SGF), C-Series Press-Pin Connector

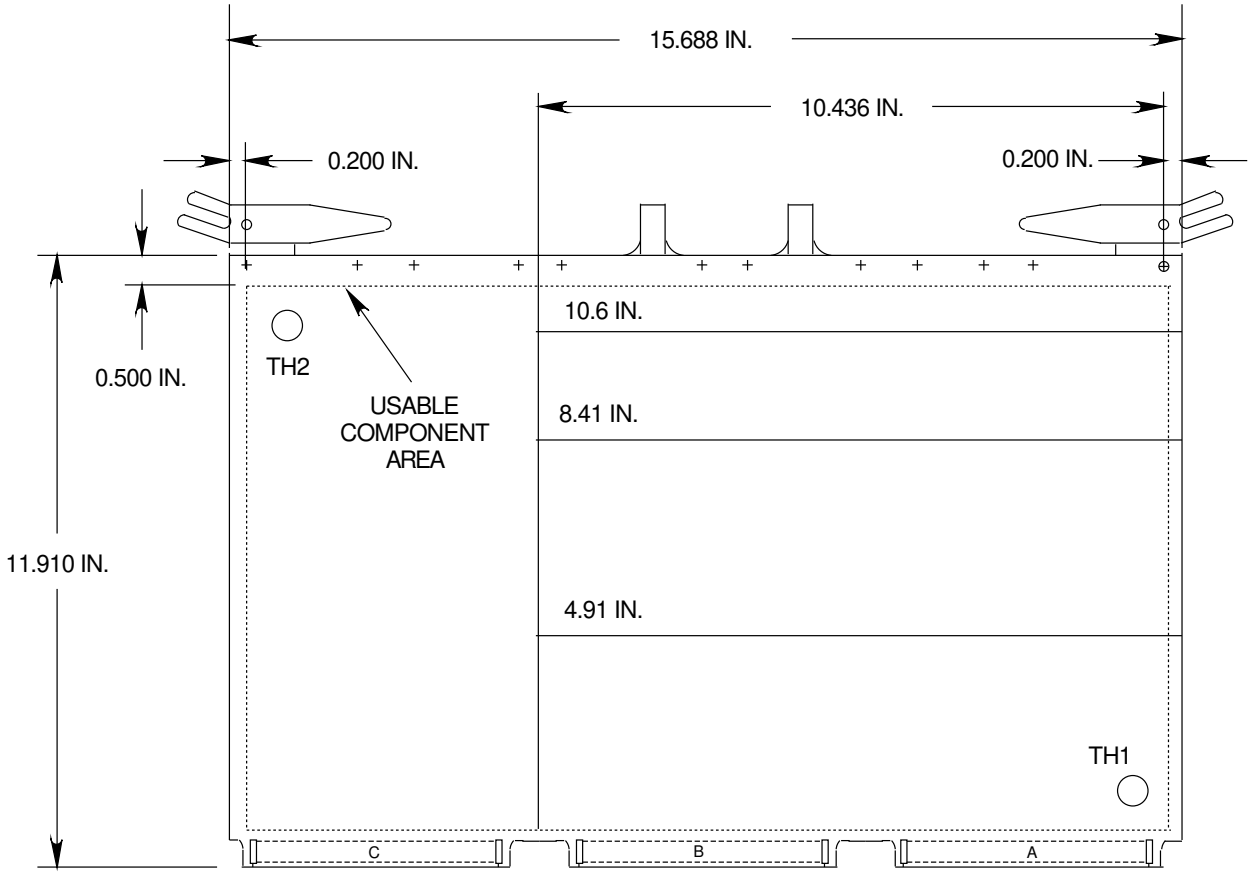


NOTE

This drawing is for reference only. Refer to E-MD-ELEN619-0-0, 620-0-0, and 621-0-0 in the PC Board Engineering Handbook for more detailed information.

Refer to subhead 4.1 and Exhibit 14.

Exhibit 11: L-series Circuit Outline (Press-Pin Connector)

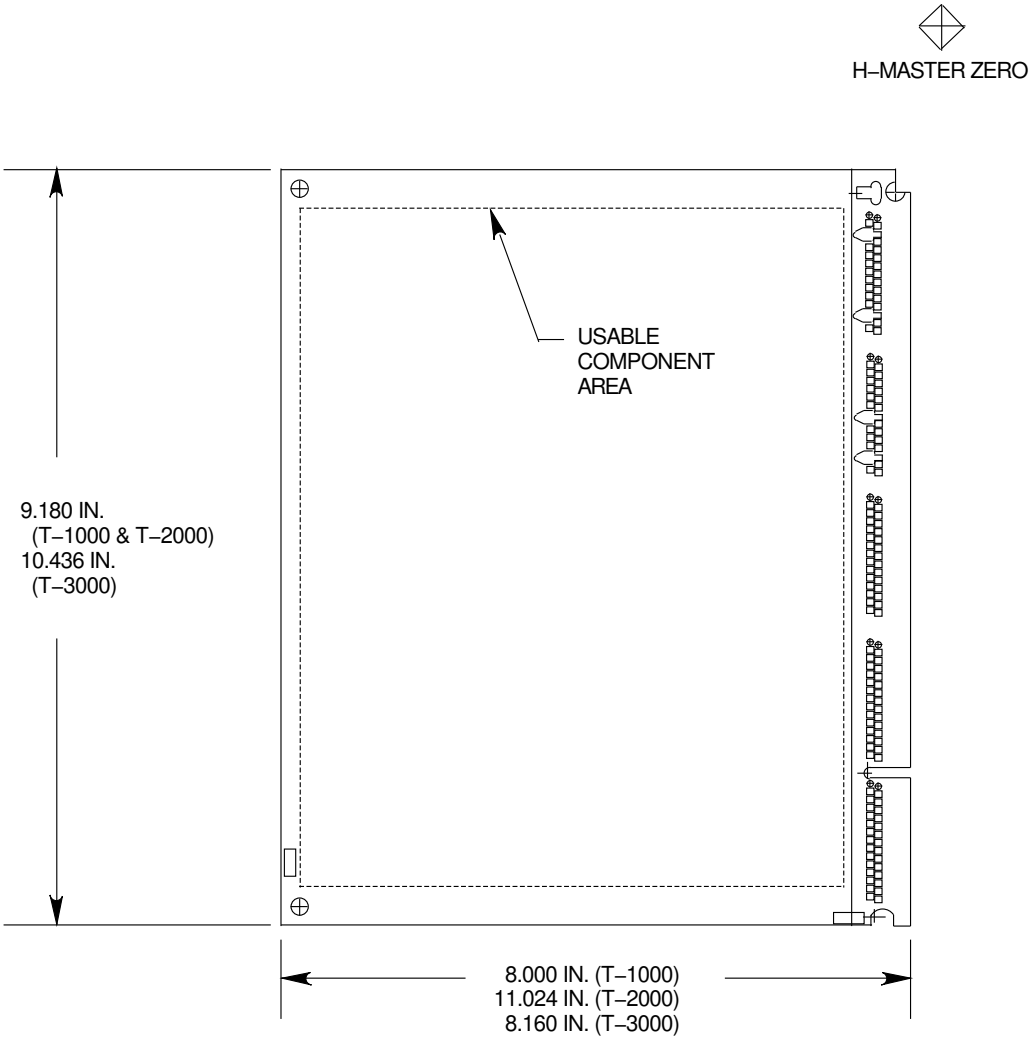


NOTE: THIS DRAWING FOR REFERENCE ONLY.
REFER TO D–MD–ELEN623–0–DBU AND
D–MD–ELEN652–0–DBU IN THE
PC BOARD ENGINEERING HANDBOOK
FOR DETAILED INFORMATION.

"H" MASTER ZERO

Refer to subhead 4.1 and Exhibit 14.

Exhibit 12: T-series Circuit Outline (ZIF Connector)



NOTE: THIS DRAWING FOR REFERENCE ONLY.
REFER TO THE FOLLOWING DRAWINGS IN
THE PC BOARD ENGINEERING HANDBOOK
FOR DETAILED INFORMATION.

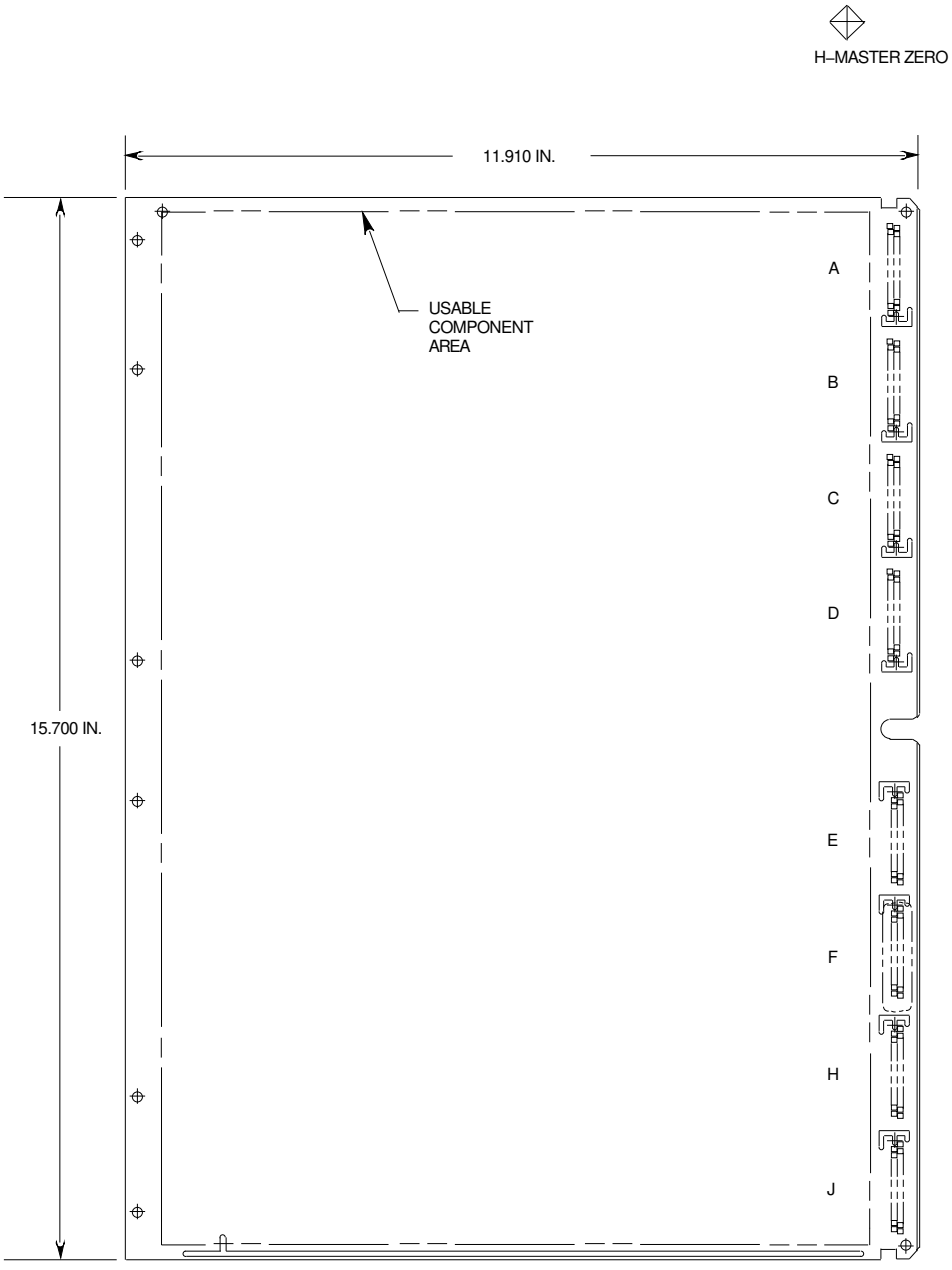
T–1000: EL–EN626–0–DBU (8.000 X 9.180), USES ZIF CONNECTOR
EL–EN634–0–DBU

T–2000: EL–EN650–0–DBU (11.024 X 9.180), USES ZIF CONNECTOR

T–3000: EL–EN653–0–DBU (8.160 X 10.436), USES 500–CONTACT 2–PIECE CONNECTOR

Refer to Exhibit 14.

Exhibit 13: F-series Circuit Outline (ZIF Connector)



NOTE: THIS DRAWING FOR REFERENCE ONLY.
FOR DETAILED INFORMATION REFER
TO D–MD–ELEN625–0–DBU IN THE
PC BOARD ENGINEERING HANDBOOK.

Refer to Exhibit 14.

Exhibit 14: Detailed Reference Drawings

CIRCUIT OUTLINES AND FINGER DETAIL DRAWINGS		ASSOCIATED ASSEMBLY BOARD DRAWING	
Document Identifier	Comments/Use	Document Identifier	Comments/Use
D-MD-ELEN601-0-0 D-MD-ELEN652-0-0	Quad circuit outline and finger detail L-series quad	D-MD-ELMF653-0-0 D-MD-ELMF654-0-0 D-MD-ELMF655-0-0	8.5-inch Quad 10.6-inch Quad 12-inch Quad (assembly board drawings)
D-MD-ELEN603-1-0	8.5-inch Hex standard circuit outline and finger detail	D-MD-ELMF656-0-0	8.5-inch Hex assembly board drawing
D-MD-ELEN603-3-0 D-MD-ELEN604-1-0 D-MD-ELEN623-0-0 D-MD-ELEN625-0-0	12-inch Hex standard circuit outline and finger detail 12-inch Comet circuit outline and finger detail 12-inch L-series module circuit outline and finger detail 12-inch F-series module circuit outline and finger detail	D-MD-ELMF658-0-0	12-inch Extended Hex assembly board drawing
D-MD-ELEN619-0-0	Standard grid fingers (C-series) circuit outline and finger detail	D-MD-ELMF665-0-0	SGF (C-series) assembly board drawing
D-MD-ELEN622-0-0	Standard fingerless circuit outline and finger detail	D-MD-ELMF659-0-0	FICS assembly board drawing
E-MD-ELEN626-0-0 E-MD-ELEN634-0-0	T-1000 series circuit outline and finger detail	D-MD-ELMF667-0-0	T-1000 series assembly board drawing
E-MD-ELEN650-0-0	T-2000 series circuit outline and finger detail	D-MD-ELMF668-0-0	T-2000 series assembly board drawing
E-MD-ELEN653-0-0	T-3000 series circuit outline and finger detail	NONE (circuits cut to size)	T-3000 series assembly board drawing

D-MD-ELENXXX-0-0 and E-MD-ELENXXX-0-0 drawings are found in EL-ENPCB-00. D-MD-ELMFXXX-0-0 drawings are found in EL-MFPCB-01, *PC Board Manufacturing Handbook - Volume 1*.

5 MODULE ASSEMBLY/TEST PROCESS RULES

Appendix D provides the insertion (onsertion) codes, lead counts, and lead pitch for surface mount components. The PACE BOM (Bill of Materials) Analysis program highlights these codes.

Use the specifications listed in Appendix C to select surface mount components. Contact Component Engineering for further information. PACE may be used to help determine current surface mount component status and availability. For further information on PACE, refer to heading 7 or contact Producibility.

Align all DIP and axial components as shown in <REFERENCE>(comp_ins_spacpos_rule_full).

Avoid hand-insertion-only parts; they can cost 20 cents versus 2 cents for machine-insertable components.

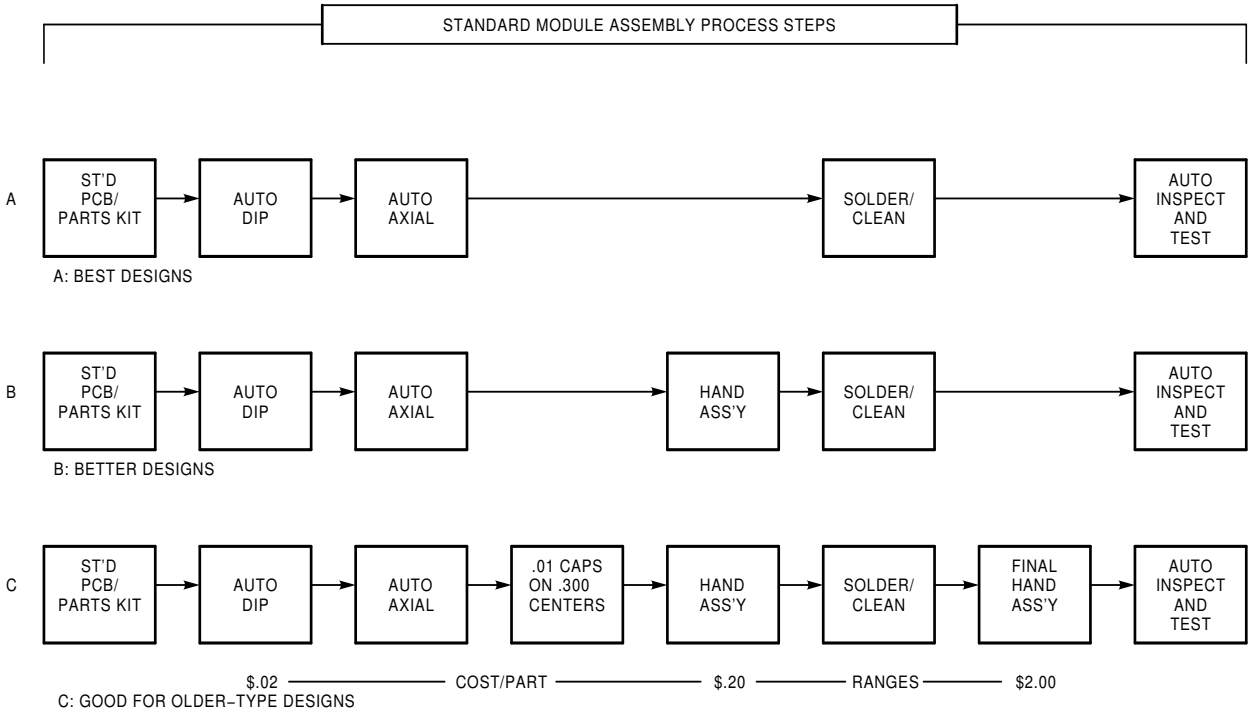
See <REFERENCE>(comp_ins_spac_fig_full) and <REFERENCE>(fics_comp_shear_fig_full) for allowable dimensions from the component body to the circuit edge.

Design circuits for testability to fit the current capabilities of diagnostic test equipment. See <REFERENCE>(section_6).

RULE 1090: OPTIMIZE DESIGN TO THE STANDARD MODULE ASSEMBLY PROCESS

When a design engineer defines a parts list, he or she has also defined the assembly process. The parts list should be engineered to take advantage of the process that requires the fewest number of steps. The process letter must be entered on the GDC code block number 8; A, B, or C must include a standard PWB technology selected from <REFERENCE>(techdef_pwbtol_fig_full) and a standard outline selected from EL-ENPCB-00. All components must have Digital part numbers and appropriate process compatibility codes as defined in the Digital standard parts book maintained by Component Engineering. Refer to Exhibit 15.

Exhibit 15: Optimum Designs Versus Manufacturing Process Steps



Note: Each step has fixed set-up, planning, and inspection costs. Enter letter A, B, or C in the PDQ Form as shown in Exhibit 3.

RULE 1100: MACHINE-INSERTABLE DIPS

In order to accommodate the machine-insertion capabilities of Digital manufacturing plants, the number of machine-insertable DIPs from <REFERENCE>(select_0300_pkg_rule_full), must be specified. Limit the number of part numbers to the following:

Best condition:	Less than 24
Good:	Less than 48
Fair:	Less than 72
Worst:	More than 72

RULE 1110: MACHINE-INSERTABLE AXIAL PARTS

Specify machine-insertable axial parts from <REFERENCE>(mach_ins_axial_fig_full). Limit quantity to less than 80 part numbers.

RULE 1130: PROCESS-COMPATIBLE COMPONENTS

Specify all components to be process compatible. Process-compatible means that no step in the assembly process will degrade the component. See the appropriate component engineer and/or Producibility for details.

RULE 1160: THROUGH-HOLE COMPONENTS - SOLDER SIDE 2

No through-hole components are allowed on solder side 2.

6 GENERAL MODULE DESIGN AND MANUFACTURING GUIDELINES

6.1 BAR CODES

If you follow the recommendations of *DEC STD 047-1 Physical Requirements for Bar Coding* for bar code labeling on a module, an area must be left free of components to allow the manufacturing plant to add the bar code label. If bar codes are used, the location must be noted on the product documentation.

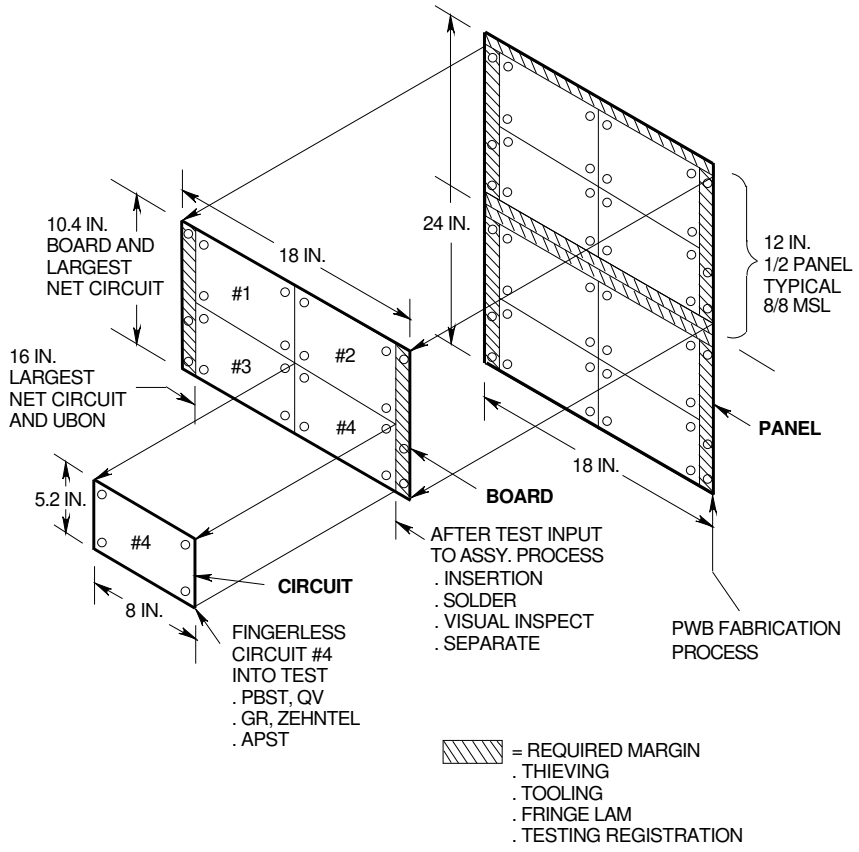
RULE 1200: BAR CODE LABEL SIZE

The minimum size for a bar code label is 0.25 inch by 4.3 inch. See either Producibility or the assembly plant engineer for bar code label sizes.

6.2 FICS (FINGERLESS CIRCUIT STANDARD) CIRCUIT/BOARD/ PANEL CONFIGURATIONS

Exhibit 16 illustrates how a circuit is stepped and repeated throughout the board fabrication assembly process.

Exhibit 16: FICS Circuit/Board/Panel Configurations



7 PRODUCIBILITY AUTOMATION AND COST ESTIMATOR (PACE) PROGRAM

PACE is a multi-function program that combines a decision-making tool used by producibility and design engineers to estimate the cost of a module assembly with an interface to a database of module producibility information. Producibility will still handle those modules that must incur the cost of nonstandard processing.

An approximation of the cost (± 20%) to produce a new module or backplane in volume may be obtained through PACE for comparative analysis. PACE should minimize time to market and new product start-up (E69) costs, as well as long-term costs. It allows designers to forecast the estimated costs of standard process choices while the design is still fluid. Several different sizes, technologies, hand versus automatic assembly options, and so forth can be compared for informed trade-offs. Features of PACE include LIFE COST comparisons, WHAT IF..., HI TECH PREVIEWS, and HELP features.

PACE also provides a means for engineers to communicate producibility information and for managers to generate reports containing data base information.

System managers should contact Kathy Bailey (SALEM::BAILEY_K) for instructions on installing PACE on their system.

APPENDIX A - MAXIMUM IC CALCULATION AND EIC EQUIVALENCES

The following formula can be used for calculating the maximum number of ICs that can be placed on a Digital printed-wiring board.

Horizontal IC Count	X = W/A
Vertical IC Count	Y = H/B

Where:

W =	Usable board width
H =	Usable board height
A =	IC pin/pin width + spacing to next IC
B =	IC pin/pin height + space to decoupling + space from decoupling to next IC

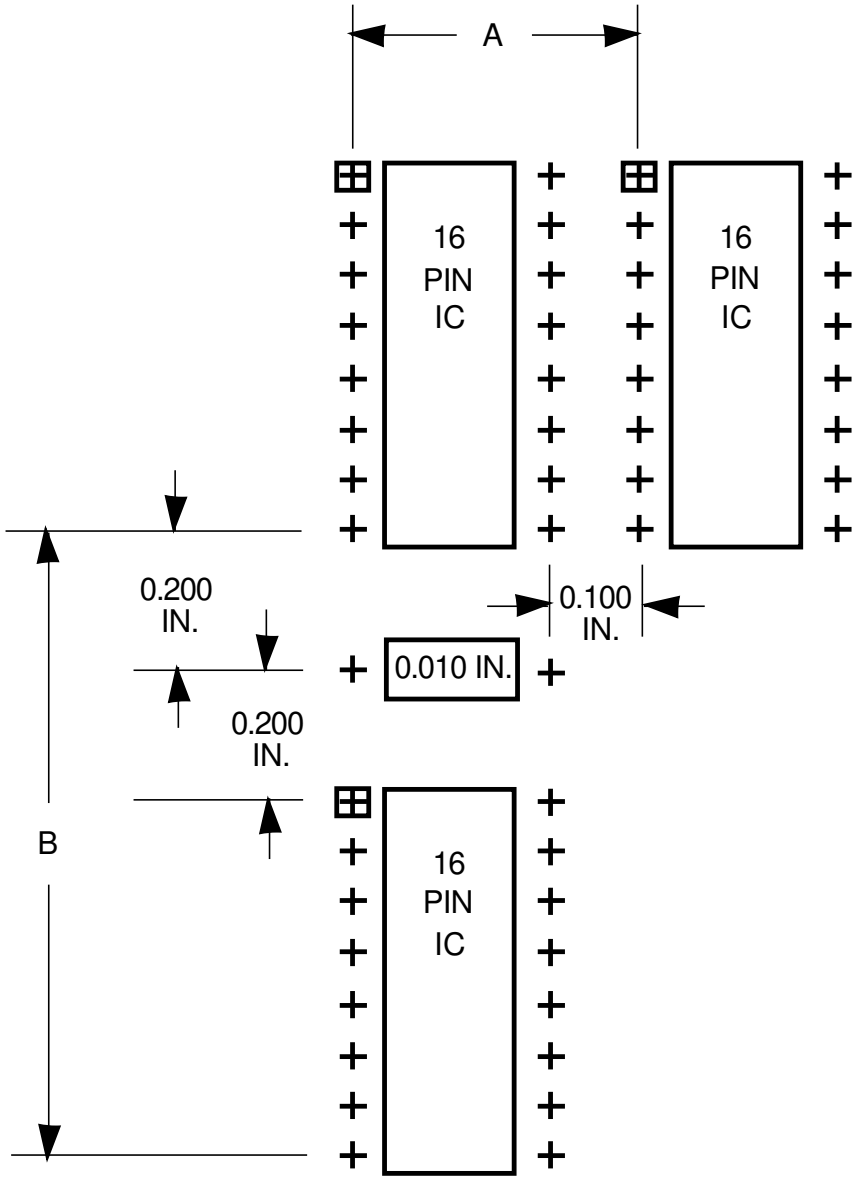
Exhibit 17 shows how to determine the distances A and B. In this figure, 16-pin ICs are used as a representative IC size. Dimensions are in inches.

Example: Standard extended hex

X =	W/A
X =	15.30/.4 = 38
X =	38 ICs wide
Y =	H/B
Y =	10.10/1.10 = 9
Y =	9 ICs high with decoupling

It is not always possible to calculate a matrix that will be filled completely with ICs. In such a case, the ICs at the end of each row (or column) that is not completely filled should be butted up close against the board edge, allowing the minimum spacing between IC and edge. The extra space should be provided within the matrix (rather than at the edges) to provide more space for routing between the rows or columns of ICs.

Exhibit 17: IC Matrix



Use the table shown in Exhibit 18 to determine EIC equivalences.

Exhibit 18: EIC Equivalences (Normalized Component Counts)

Qty.	Description	Normalized Component
1	14–Pin IC 0.3–Inch Centers	= 1.0
1	16–Pin IC 0.3–Inch Centers	= 1.1
1	18–Pin IC 0.3–Inch Centers	= 1.3
1	20–Pin IC 0.3–Inch Centers	= 1.4
1	22–Pin IC 0.4–Inch Centers	= 1.7
1	24–Pin IC 0.4–Inch Centers	= 2.0
1	24–Pin IC 0.6–Inch Centers	= 3.0
1	28–Pin IC 0.6–Inch Centers	= 3.7
1	28–Pin IC 0.9–Inch Centers	= 5.4
1	40–Pin IC 0.6–Inch Centers	= 4.7
1	¼–Watt Resistor Carbon Film	= 0.167
1	½–Watt Resistor Carbon Film	= 0.33
1	1–Watt Resistor Carbon Composition	= 0.7
1	2–Watt Resistor Carbon Composition	= 1.0
1	Diode (0.4–Inch Length X 0.1–Inch Diameter	= 0.167
1	Capacitor 0.047 µF (0.4–Inch X 0.1–Inch Diameter)	= 0.167
1	Capacitor Decoupling	= 0.167
1	Capacitor 1 pF – 1,000 pF	= 0.20
1	Capacitor 6.8 µF	= 0.33
1	Transistor TO–3 Case	= 3.0
1	Transistor TO–5 Case	= 0.4
1	Transistor 0.25–Inch Diameter or Less	= 0.2
1	10–Pin Berg	= 3.0
1	20–Pin Berg	= 4.0
1	40–Pin Berg	= 6.0

NOTE

To determine normalized component counts for miscellaneous components and for ICs not listed above, count each 0.3 square inch of component as one normalized component.

APPENDIX B - CURRENT CARRYING CAPACITIES

The chart shown in Exhibit 19 shows the recommended conductor width/thickness necessary to carry specific current loads. Note that the variable involved is the temperature rise above ambient. The acceptable temperature rise can only be determined by Engineering; therefore, it is strongly suggested that the engineer be totally involved when it becomes necessary to use this chart. Refer to MIL STD 275E *Printed Wiring for Electrical Equipment* for further information.

NOTE

The maximum allowable temperature must not exceed 130 degrees C for double-sided power supply designs and 105 degrees C for multilayer designs. Refer to <REFERENCE>(sec2_intro_head_full) and <REFERENCE>(prodsafrul_fig_full).

Application Notes, Exhibit 19

1. The chart in Exhibit 19 helps estimate temperature rises (above ambient temperature) versus current for various cross-sectional areas of etched copper conductors. It is assumed that normal design conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves shown in the chart include a normal 10 percent de-rating current carrying capability of the etch to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.
2. Additional de-rating of 15 percent with respect to current is suggested under the following conditions:
   a. For panel thickness of 1/32 inch or less
   b. For conductor thickness of 0.0042 inch (3 oz/sq ft)
3. For general use the permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate and the maximum ambient temperature where the panel will be used.
4. For single conductor applications, the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.
5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-sections of the parallel conductors. The equivalent current is the sum of the currents in the conductors.
6. The effect of heating due to attachment of power-dissipating parts is not included.
7. The conductor thicknesses in the chart do not include conductor overplating with metals other than copper.

Exhibit 19: Conductor Cross-Section in Square Mils

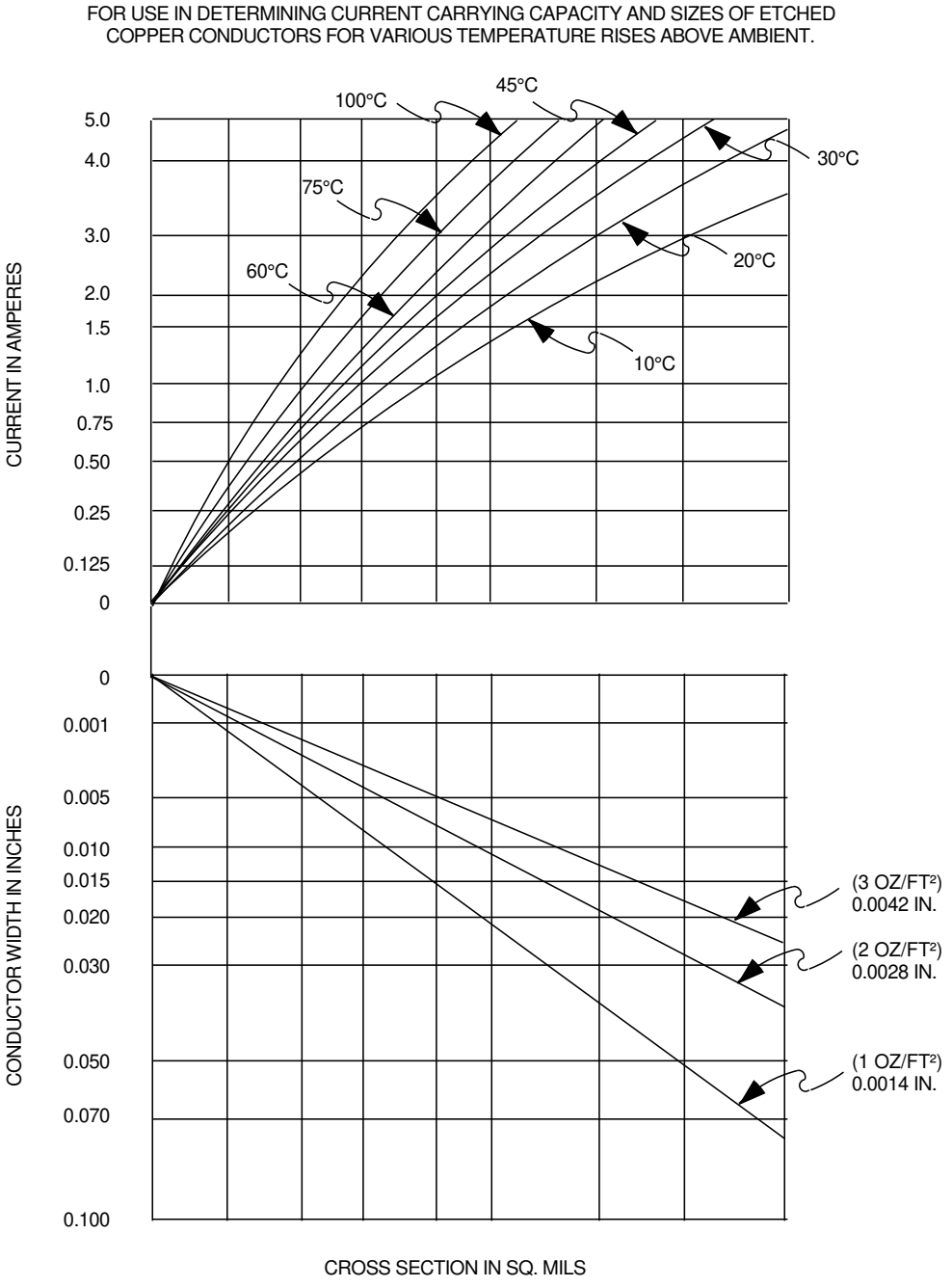


Exhibit 20: Typical Conductor Width/Thickness for PWBs

Conductor Type	Width (inch)	Foil Thickness Ounces (inch)	Plated Ounces (inch)
Signal (O.L.– Pwr. Supplies)	0.020 min	2 oz (0.0028)	3 oz (0.0042)
Signal (O.L.)	0.015 min	1 oz (0.0014)	2 oz (0.0028)
Signal (O.L.)	0.006 min	1/2 oz (0.0007)	1.5 oz (0.0021)
Signal (I.L.)	0.006 min	1 oz (0.0014)	—
Power/Ground Plane (See Note)	0.030 min 0.030 min	1 oz (0.0014) 2 oz (0.0028)	— —

NOTE

For further information on power/ground plane minimums, refer to <REFERENCE>(cu_power_plane_rule_full).

Exhibit 21: Current Carrying Capacities of PWB Copper Etch

Plating Density Cu.Wt/Sq.Ft.	Current Rating (DC Amperes)			Temperature Rise (C)
	0.010–Inch Via		0.010–Inch Dispersion Etch	
	Int.	Ext.	Ext.	
1 oz	1.1 1.5 1.9 2.1	2.1 3.0 3.7 4.0	0.75 1.1 1.3 1.5	10 20 30 45
2 oz			1.3 1.7 2.1 2.5	10 20 30 45
3 oz			1.75 2.25 3.0 3.5	10 20 30 45

APPENDIX C - SUMMARY OF TYPICAL SURFACE MOUNT FEATURES

The chart in Exhibit 22 shows the major features defined during the development of surface mount technology within Digital, and is shown for reference only. For detailed descriptions of each technology level, refer to EL-MF417-02. Contact your producibility engineer for assistance in selecting the proper technology level. Exhibit 23 compares the major features of each surface mount technology level.

Exhibit 22: Summary of Typical Surface Mount Features

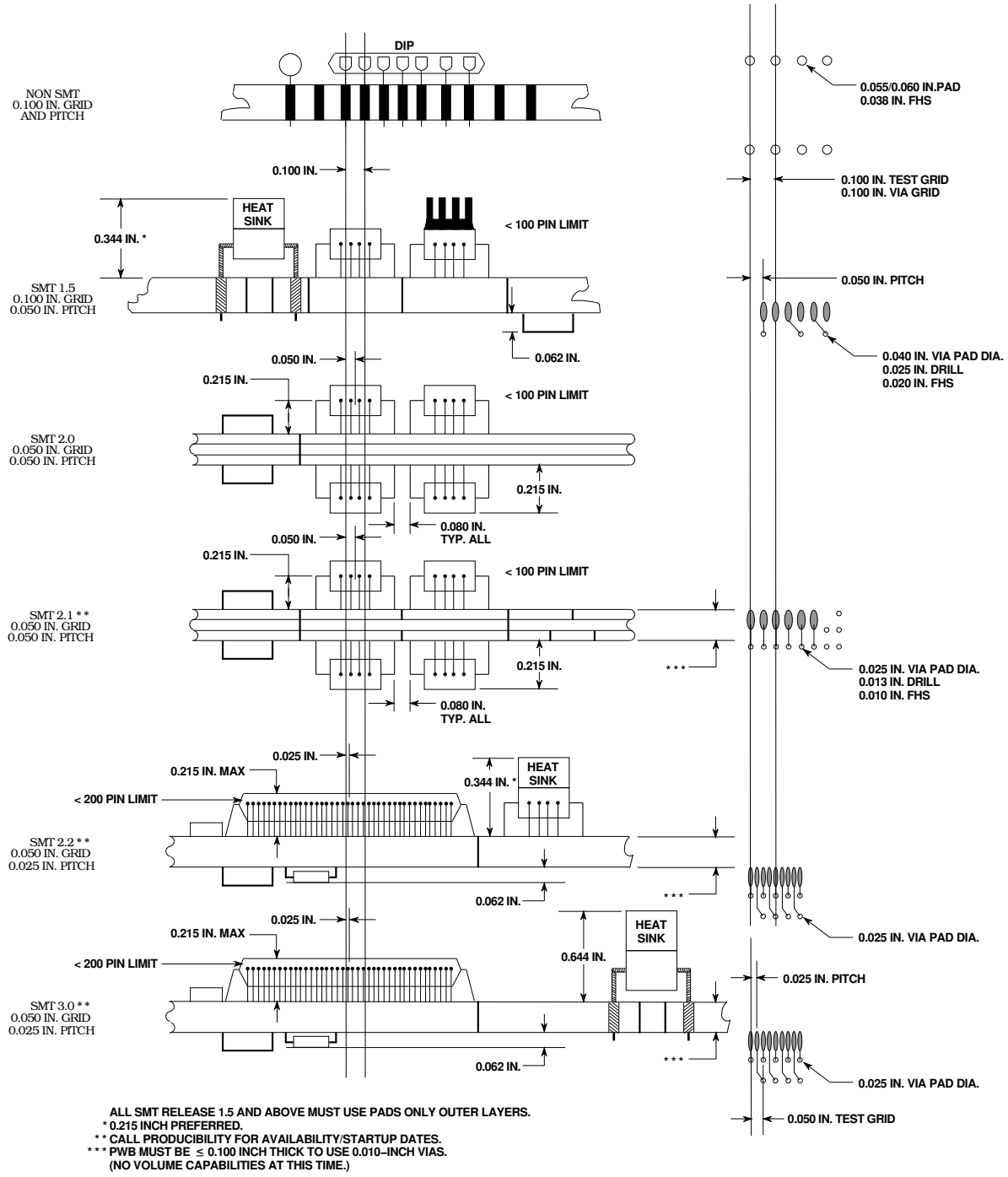
DEC STD 030 MODULE MANUFACTURING MINIMUM DESIGN FEATURES FOR SMT									
COMPONENTS		PRINTED–WIRING BOARD		MODULE ASSEMBLY		MODULE TEST		MAJOR FEATURE	
PIN COUNTS	SMT USE PITCH TYP	LBV OR PTH (FHS/PAD) (SEE NOTE 4)	VIA/TEST GRID LINE WIDTH/ SPACE	SIDE 1 THRU TYPE SMT PADS SMT ACTIVE	SIDE 2 SMT PADS SMT ACTIVE	TEST GRID VIA TEST PAD TEST PAD (SEE NOTE 8)	MAX HEIGHT SIDE 1/SIDE 2 OUTLINE (SEE NOTE 5)		
	N/A	PTH 0.038/0.060	0.100/0.100 0.006/0.010	DIP THRU LEAD	N/A	0.0100 0.055 OR 0.060	0.344/0.062 16 X 12	NON SMT	
	0.050 SIDE 1 ONLY	PTH 0.020/0.040 NO PAD LAYER	0.100/0.050 0.006/0.010	MIXED MOUNT (FEW CHIP)	N/A	0.0100 0.055 OR 0.060	0.344/0.062 0.215/NA 16 X 12	0.5	TECHNOLOGY LEVEL
	0.050 SIDE 1 ONLY	PTH 0.020/0.040	0.100/0.050 0.006/0.010	MIXED MOUNT	N/A	0.100 0.040 MIN	0.344/0.062 16 X 12	1.0	
	0.050 SIDE 1 PASSIVES SIDE 2	PTH 0.020/0.040	0.100/0.050 0.006/0.010	MIXED MOUNT	NO THRU SMT PASSIVE ONLY	0.100 0.040 MIN	0.344/0.062 16 X 12 (SEE NOTE 2)	1.5	
	0.050 BOTH SIDES	PTH 0.020/0.040	0.100/0.050 0.006/0.010	SMT PASSIVE ACTIVES	NO THRU SMT PASSIVE ACTIVES	0.100 0.040 0.040	0.215/0.215 8 X 10.4	2.0	
	0.050 BOTH SIDES	PTH LBV 0.010/0.025 (SEE NOTE 7)	0.050/0.050 0.005/0.005	SMT PASSIVE ACTIVES	NO THRU SMT PASSIVE ACTIVES	0.050 0.035 MIN 0.035 (SEE NOTE 6)	0.215/0.215 8 X 10.4	2.1 (SEE NOTE 1)	
	0.025 SIDE 1 PASSIVES SIDE 2	PTH 0.010/0.025 (SEE NOTE 7)	0.050/0.050 0.005/0.005 (SEE NOTE 3)	SMT PASSIVE ACTIVES	NO THRU SMT PASSIVE ONLY	0.050 0.035 MIN 0.035 (SEE NOTE 6)	0.344/0.062 8 X 10.4 (SEE NOTE 2)	2.2 (SEE NOTE 1)	
28–PIN CLCC 68–PIN J–BEND 224–PIN GULLWING CHIP CARRIERS	0.025 SIDE 1 PASSIVES SIDE 2	PTH 0.010/0.025 (SEE NOTES 7 AND 9)	0.050/0.050 0.005/0.005 (SEE NOTES 3 AND 9)	MIXED MOUNT SIDE 1 PASSIVES ACTIVES	NO THRU SMT PASSIVES SMT ACTIVES SIDE 2	0.050 0.035 MIN 0.035 (SEE NOTE 6)	0.640/0.215 16 X 12	3.0 (SEE NOTE 1)	

Notes:

1. Call Producibility for availability/start-up dates.
2. 0.215-inch preferred.
3. Bare board test coverage with 0.025-inch pitch footprint pads is limited -see <REFERENCE>(drill_bareboard_rule_full).
4. See <REFERENCE>(etch_inlayer_smt_rule_full) for recommendations for via and pad sizes.
5. Refer to <REFERENCE>(maxhi_plugin_rule_full).
6. Vias chosen as test points will be expanded by the design software using the VLS soft tool STP.
7. PWB must be $\leq$ 0.100-inch thick to use 0.010-inch vias. (No volume capabilities at this time.)
8. Refer to <REFERENCE>(testpad_size_rule_full).

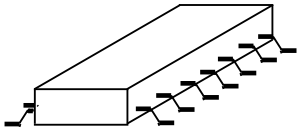
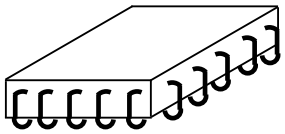
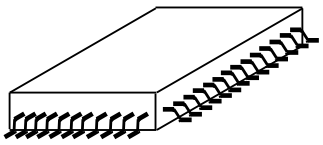
9. Controlled impedance characteristics (see <REFERENCE>(impede_testgen_rule_full) through <REFERENCE>(impede_testprobe_rule).)

Exhibit 23: Comparison of Major Surface Mount Technology Levels



ALL SMT RELEASE 1.5 AND ABOVE MUST USE PADS ONLY OUTER LAYERS.
* 0.215 INCH PREFERRED.
* * CALL PRODUCIBILITY FOR AVAILABILITY/STARTUP DATES.
* * * PWB MUST BE ≤ 0.100 INCH THICK TO USE 0.010–INCH VIAS.
(NO VOLUME CAPABILITIES AT THIS TIME.)

APPENDIX D - INSERTION (ONSERTION) CODES, LEAD COUNTS, AND LEAD PITCH BY PART CATEGORY

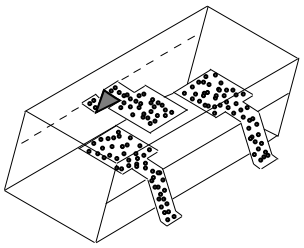
Package Category	Insertion (Onsertion) Code	Package Name	Lead Count	Lead Type *	Lead Pitch (Inch)	Package Material
SOICs (Small Outline IC) 	BB	SOIC8	8	G	0.050	Plastic
	BC	SOIC14	14	G	0.050	Plastic
	BD	SOIC16	16	G	0.050	Plastic
	BE	SOIC16L	16	G	0.050	Plastic
	BF	SOIC20	20	G	0.050	Plastic
	BG	SOIC24	24	G	0.050	Plastic
	BH	SOJ26	20/26	J	0.050	Plastic
	BI	SOIC28	28	G	0.050	Plastic
PLCCs (Plastic Leaded Chip Carrier) 	DA	RES 16	16	J	0.050	Plastic
	DB	PLCC18AA	18	J	0.050	Plastic
	DC	PLCC18LG	18	J	0.050	Plastic
	DD	PLCC20	20	J	0.050	Plastic
	DE	PLCC28	28	J	0.050	Plastic
	DF	PLCC44	44	J	0.050	Plastic
	DG	PLCC68	68	J	0.050	Plastic
	DH	PLCC84	84	J	0.050	Plastic
	DI	FLIO132	132	G	0.025	Plastic
	DJ	FLIO164	164	G	0.025	Plastic
	DK	PLCC32	32	J	0.050	Plastic
CLCCs (Ceramic Leaded Chip Carrier) 	EF	CLCC44	44	G	0.050	Ceramic
	EG	CLCC68	68	G	0.050	Ceramic
	EH	CLCC84	84	G	0.050	Ceramic
	EI	FLIO132	132	G	0.025	Ceramic
	EJ	FLIO164	164	G	0.025	Ceramic

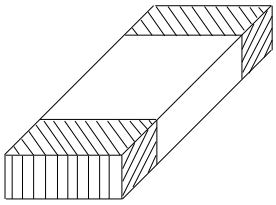
* Lead Types –– G = Gull–Wing, J = J–Bend, L = Leadless

NOTE

Appendix D is FOR REFERENCE ONLY. For detailed information, refer to EL-MF228-00, *Component Categories and Codes for Machine and Non-Machine Insertable Components*.

INSERTION (ONSERTION) CODES, LEAD COUNTS, AND LEAD PITCH BY PART CATEGORY (Continued)

Package Category	Insertion (Onsertion) Code	Package Name *	Lead Count	Lead Type **	Lead Pitch (Inch)	Package Material
Others 	OA OB OC OD	SOT23 SOT89 POT25 OSC A	3 3 3 4	G G G J		Plastic Plastic Ceramic

Package Category	Insertion (Onsertion) Code	Package Name	Component Assignments
Chips (Passive) 	CA	0805	Cer_Cap
	CB	1005	–
	CC	1206	Cer_Cap 1/4 wRes
	CD	1210	Cer_Cap 1/4 wRes
	CE	1505	–
	CF	1805	–
	CG	1812	Cer_Cap
	CH	1825	Cer_Cap
	CI	2218	–
	CJ	2225	–
	CK	2622	–
	CL	LQN3N	Inductor
	CO	2512	1.5w Res
	CT	CASE A	Tant_Cap
	CU	CASE B	Tant_Cap
	CV	CASE D	Tant_Cap
	CW	CASE E	Tant_Cap
	CX	CASE F	Tant_Cap
	CY	CASE G	Tant_Cap
	CZ	CASE H	Tant_Cap

* SOT = Small Outline Transistor/HMS–Series Diode
* POT = Small Outline Potentiometer
* OSC = Small Outline Oscillator
** Lead Types –– G = Gull–Wing, J = J–Bend, L = Leadless

NOTE

Insertion Codes appear in the Manufacturing Data Base and are *not* used in Digital's Part Number Format. For information on Digital part numbers, see *DEC STD 012-0 Part Identification Standard*.

REFERENCED DOCUMENTS

EL-Class Digital Documents

EL-Class Number	Document Title
EL-00012-00	*DEC STD 012-0 Part Identification Standard*
EL-00016-00	*DEC STD 016-0 Printed-Wiring Manufacturing Terminology*
EL-00030-02	*DEC STD 030-2 Module Manufacturing Standard - Product Safety Requirements*
EL-00030-04	*DEC STD 030-4 Module Manufacturing Standard - Printed-Wiring Board Design Requirements*
EL-00030-05	*DEC STD 030-5 Module Manufacturing Standard - Module Assembly and Component Insertion Rules*
EL-00030-06	*DEC STD 030-6 Module Manufacturing Standard - Module Testability Rules*
EL-00047-01	*DEC STD 047-1 Physical Requirements for Bar Coding*
EL-00066-02	*DEC STD 066-2 Waivers to Digital Design Standards*
EL-00140-01	*DEC STD 140-1 Documentation Requirements for Printed-Wiring Boards, Modules, and Backplanes*
EL-00176-00	*DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*
EL-ENPCB-00	*PC Board Engineering Handbook*
EL-MF228-00	*Component Categories and Codes for Machine and Non-Machine Insertable Components*
EL-MF417-02	*Surface Mount Technology Reference Manual - Volume 2*
EL-MFPCB-01	*PC Board Manufacturing Handbook - Volume 1*

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

Other Documents

	Document Title
	Automated CDQ Form
	Automated PDQ Form
	Module Waiver Form

Automated CDQ, PDQ, and Module Waiver forms are available from Site Producibility Engineers.

Document Number	Document Title
MIL STD 275E	*Printed-Wiring for Electrical Equipment*

Copies of Federal Standards and Military Standards and Specifications are available from the Naval Publications and Forms Center 5801 Tabor Avenue, Philadelphia, PA 19120, telephone (215) 697-3321.

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